Application of SiC Hybrid Discrete in Photovoltaic and Energy Storage Systems

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Introduction

With the increasing competitive pressure on the costs of PV and ESS, more and more customers are choosing discrete. However, replacing hybrid modules with IGBT discrete will lead to increased losses. Replacing hybrid modules with SiC MOSFETs will cause the body diode to heat up severely and be prone to failure. Therefore, this article introduces the application of SiC hybrid discrete devices. This approach can reduce loss-es while meeting cost requirements.

Introduction to discrete packaging

With the increasing switching speeds of modern IGBTs and the adoption of SiC MOSFETs, traditional 3-pin (gate, source, drain) discrete packaging can no longer meet the demands for low-noise, high-efficiency operation. As shown in **Fig.1**.

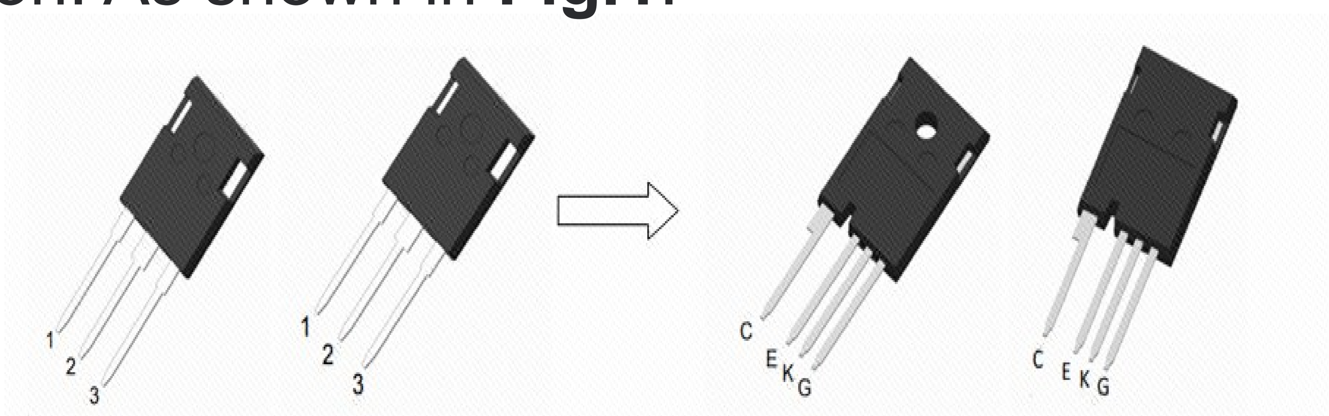

Fig. 1 Changes in Packaging of Discrete

The Kelvin pin mitigates the adverse effects of parasitic inductance (Ls) and resistance (Rs) in the main source loop, which arise due to high di/dt during fast switching transitions.This configuration offers two key ad-vantages:

a. Enhanced Switching Speed: The reduced impedance in the gate drive loop allows for faster charging/discharging of the gate capacitance (Ciss), enabling sharper turn-on/off transitions. The variation in switching speed is shown in **Fig 2**.

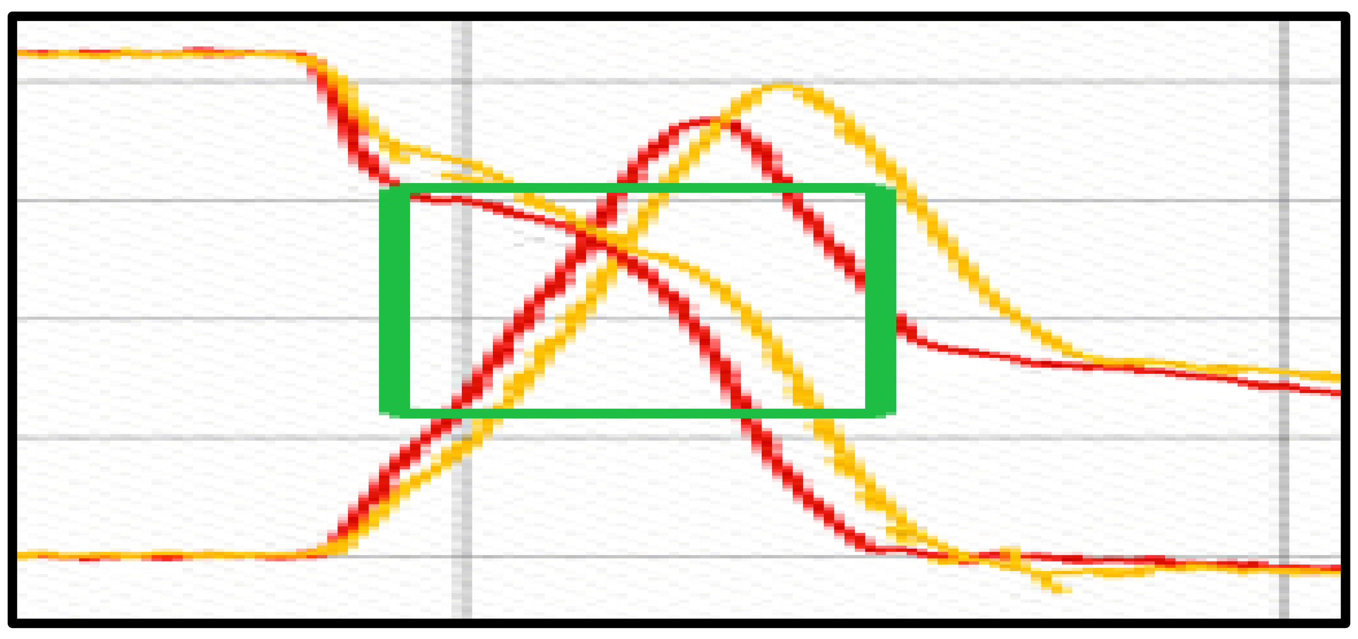

Fig 2. The variation in switching speed

b. Suppressed Gate Oscillations: By minimizing feedback interference from the power loop, the Kelvin pin dampens high-frequency ringing in VGS, improving signal integrity and reducing electromagnetic interference (EMI). The comparison of the drive waveforms be-fore and after the encapsulation change is shown in **Fig. 3**.

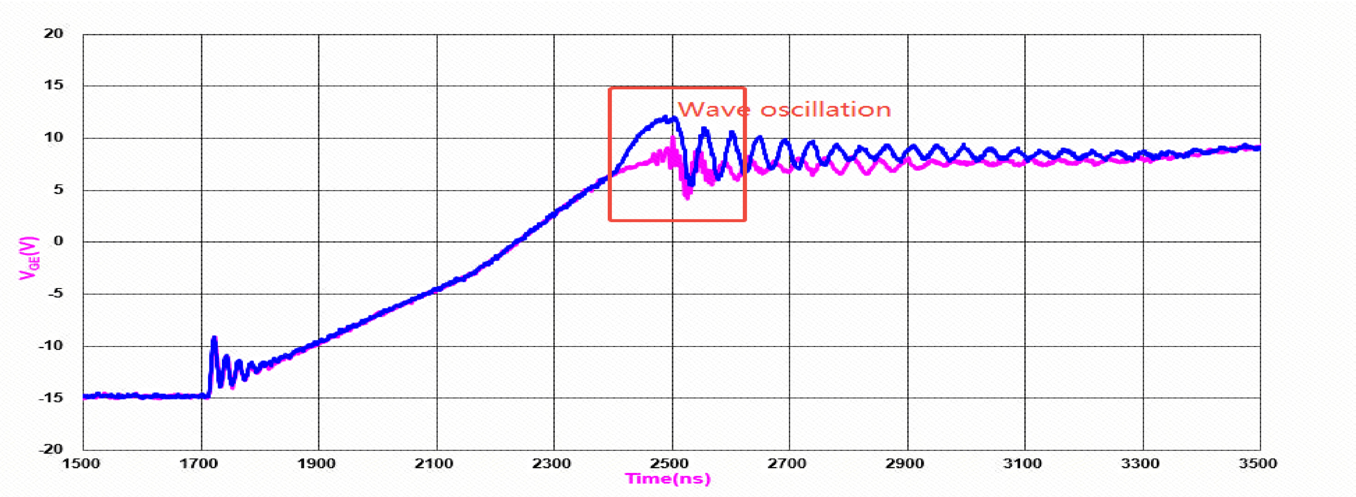

Fig.3 Comparison of the driving waveforms before and after the Kelvin pin

The application of hybrid discrete in PV

◆ Short-circuit protection application

In photovoltaic inverters, maximum power point tracking (MPPT) is now beginning to use SIC MOSFET discrete. However, this is prone to fail when the installation workers make operational mistakes. See **Fig.4** below for illustration.

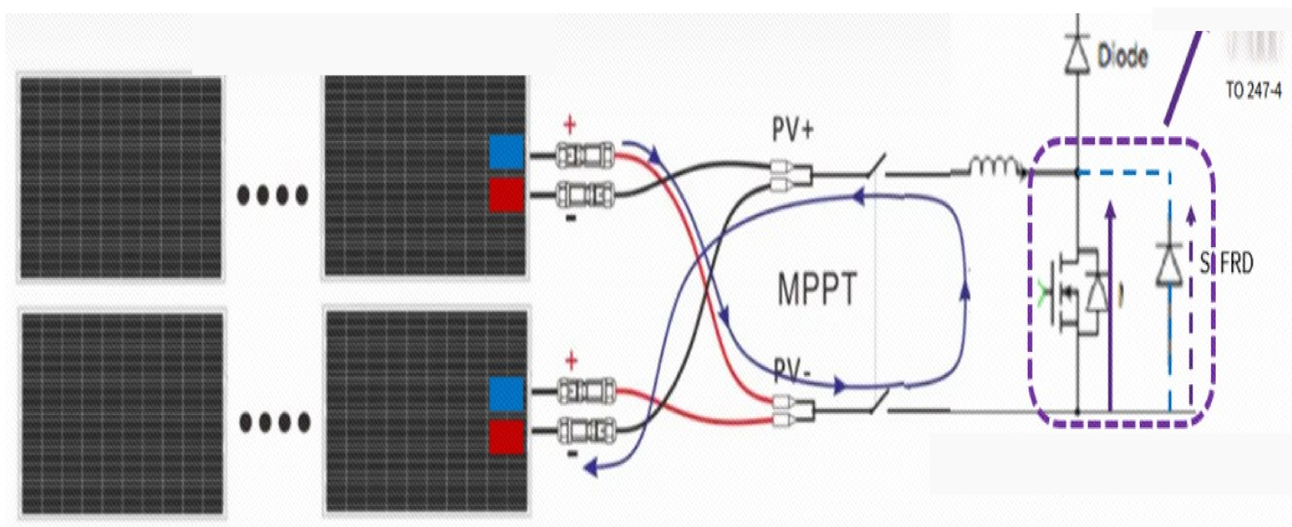

Fig.4 MPPT Front-End Short Circuit Diagram

The body diode VF of SIC MOS is relatively large. Therefore, to prevent the failure of the device when connected with reverse polarity, a diode needs to be connected in parallel. The relationship diagram of VF-IC is shown in **Fig.5**.

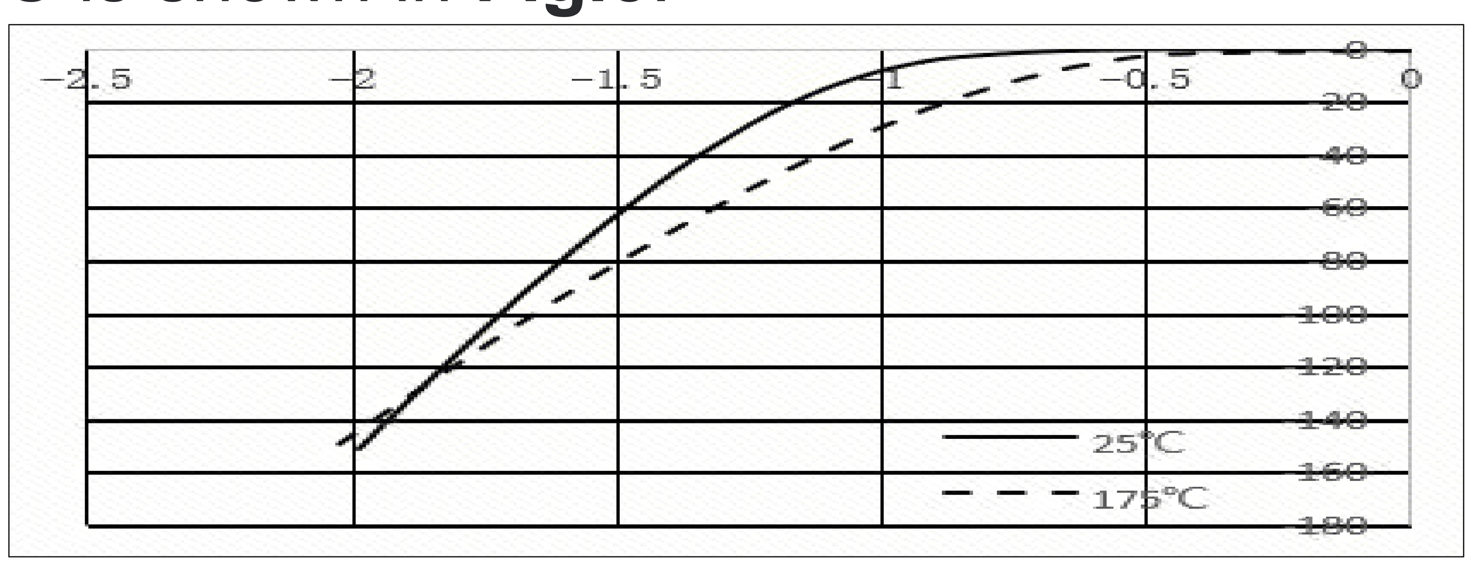

Fig. 5 FRED V-I curve

The short-circuit temperature rise of FRED is calculated by the following formula:

$$P=V*I=1.3*40=52W;$$

$$\Delta Tj=P*Rthj\text{-}c=52*0.71=36.92℃$$

Assuming an ambient temperature of 50℃, a temperature rise of around 37℃ will not cause the device to fail.

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◆Ground surge protection

The requirements for surges are stipulated in IEC6100-4-5. MPPT needs to comply with the following test standards:

Test parameter Tc = 85℃. Surge current: 10KA, Line-PE, short-circuit current waveform 8/20us. Number of times: 5 times, each interval 1 minute. Equipment requirements: Imax = 2000A@ sine, total duration 60us.

The test waveform is shown in **Fig.6**.

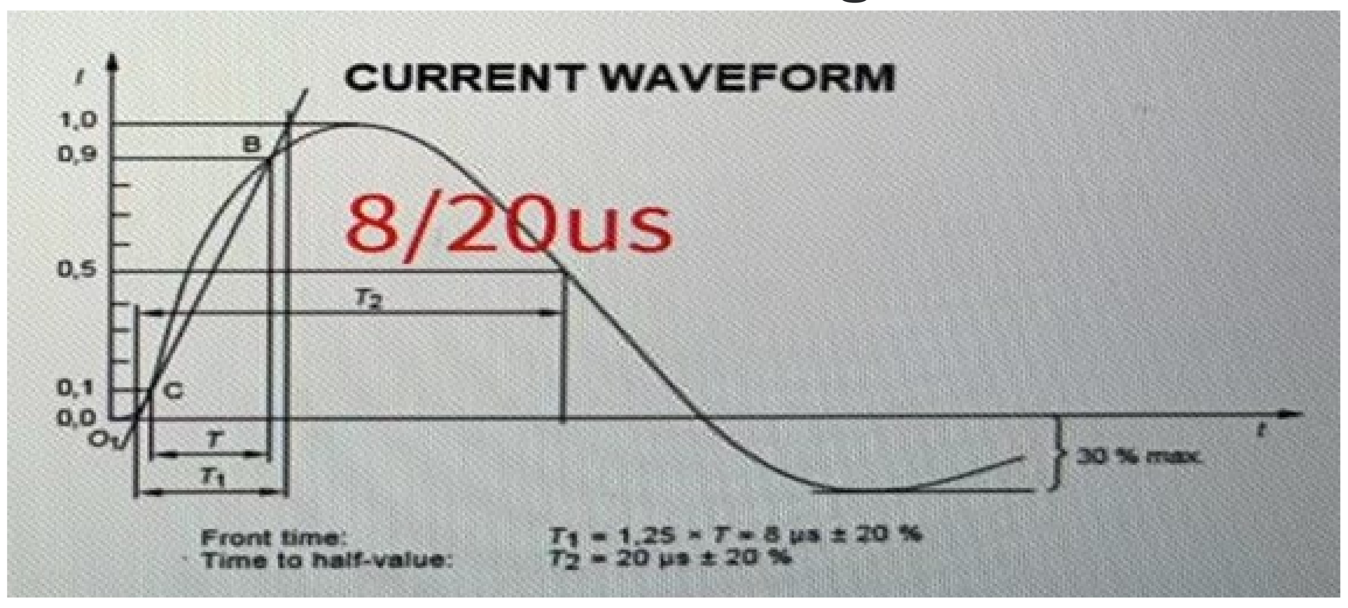

Fig. 6 Surge demand waveform

This surge capability requirement makes SiC MOS body diodes unsuitable for the application. Therefore, the use of a single tube with the inte-gration of FRED and SIC MOS is particularly important.

The application of hybrid discrete in ESS

Take the application of NPC-T in 125KW PCS as an example. The specific usage of each hybrid discrete is shown in **Table 1**. The circuit is shown in **Fig. 7**.

Table 1 125KW hybrid discrete usage

Unit	Hybrid discrete	Quantity
T1/T4	75A 1200V IGBT + 40A 1200V SIC SBD	6
T2/T3	75A 650V IGBT + 40A 650V SIC SBD	6

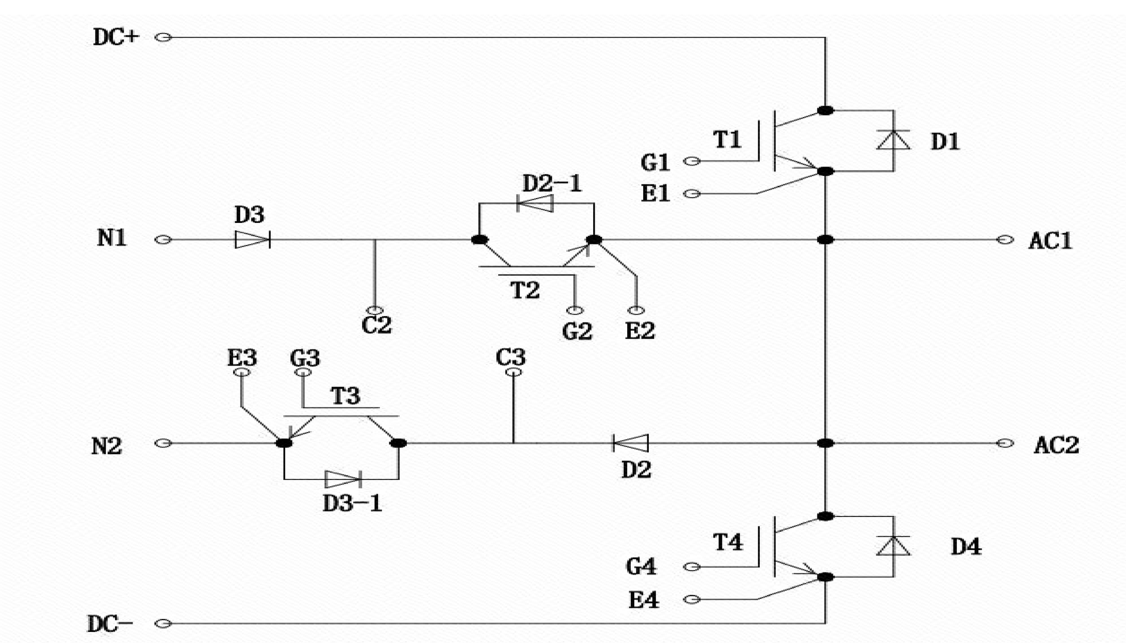

Fig. 7 NPC-T circuit topology

Compared with the FRED corresponding to 75A in the single-tube configuration, the comparison of on-state loss and efficiency is shown in **Fig. 8**.

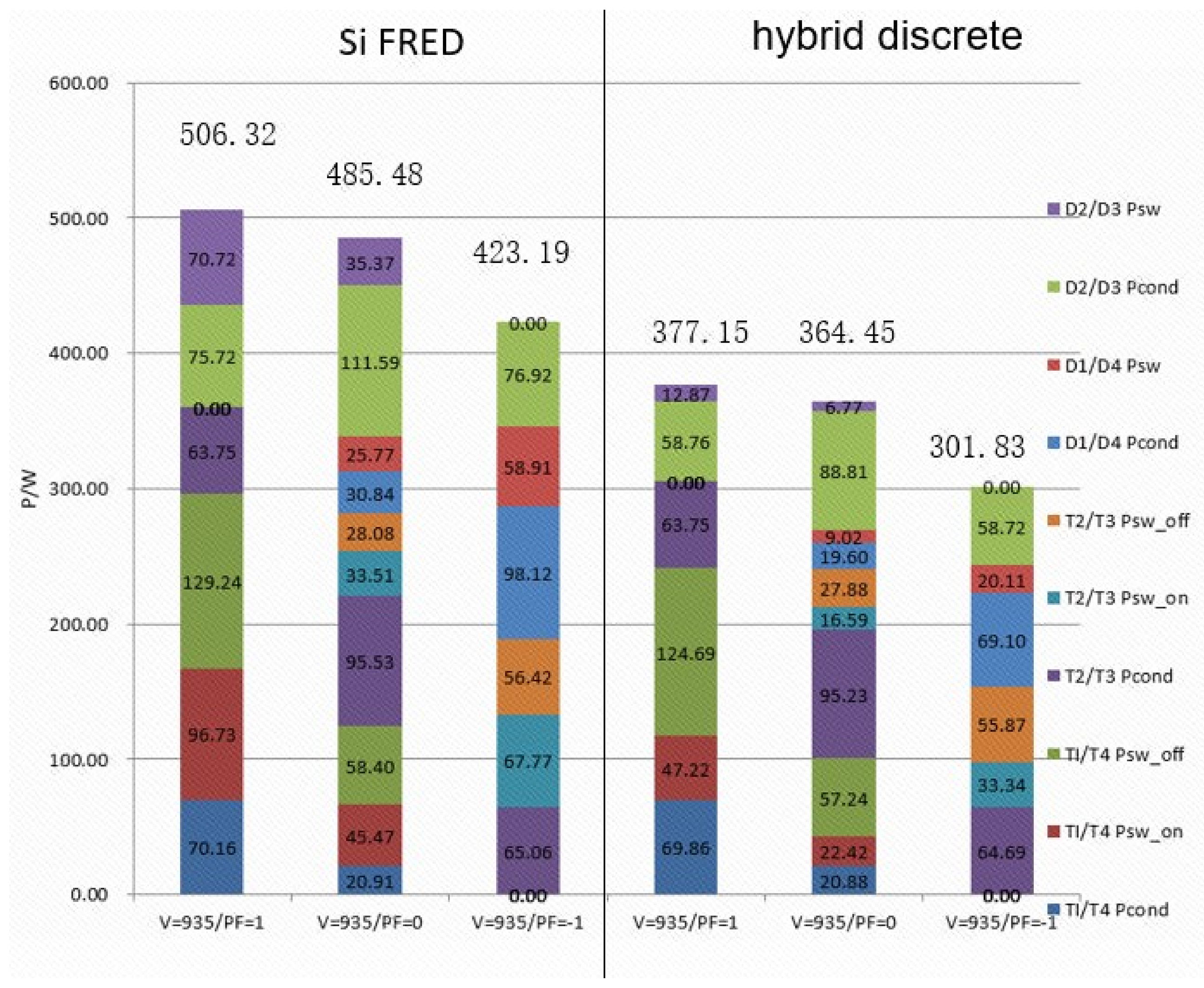

Fig. 8 Comparison of Losses between Hybrid SiC SBD and FRED

Through the full-load operation of the entire machine, it was measured that the overall efficiency increased by 0.58%, which is in good agreement with the simulation data. The picture of the entire machine is shown in **Fig. 9**.

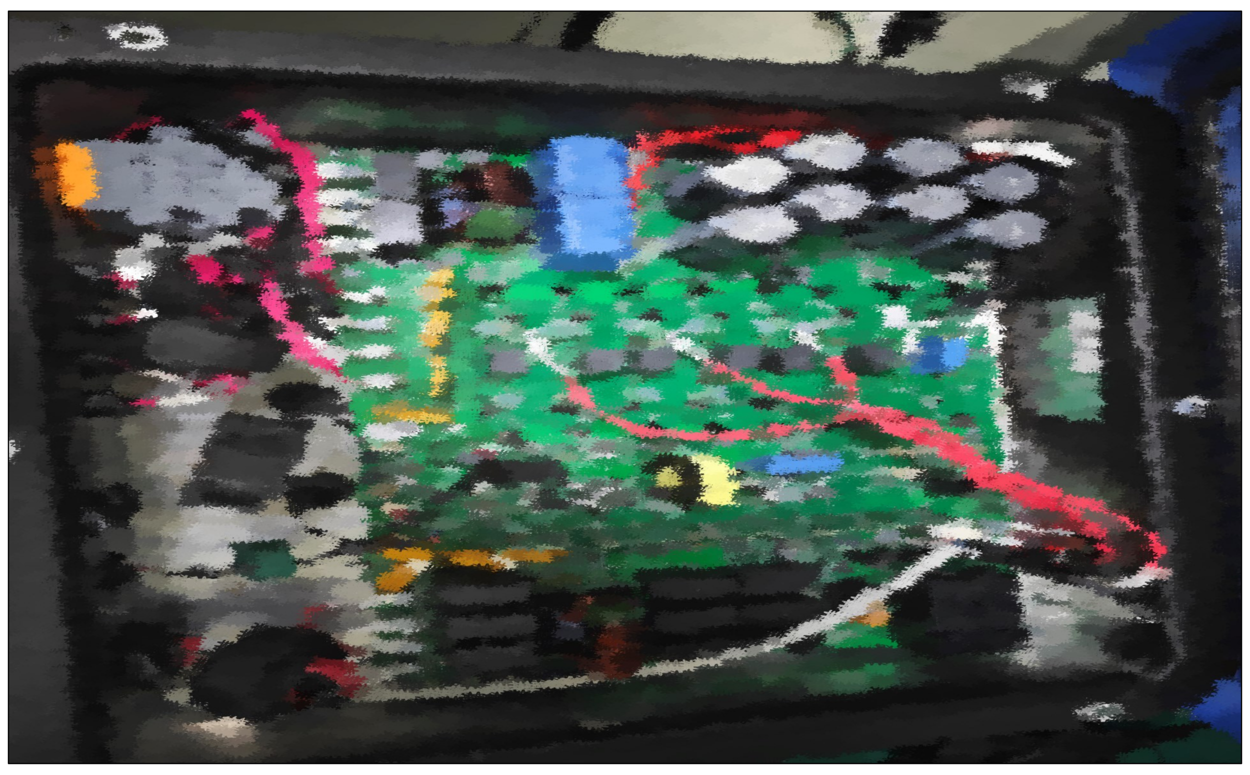

Fig. 9 Experimental verification of the entire machine image

Summary

Hybrid discrete power devices demonstrate significant advantages in both system protection and efficiency optimization. These devices exhibit enhanced robustness against current surges, and thermal runaway, thereby improving system reliability under fault conditions. Experimental results confirm a total power loss reduction of 18–22% compared to conventional designs, with particularly stable performance and minimal efficiency degradation in high-frequency switching applications ranging from 20 kHz to 50 kHz.