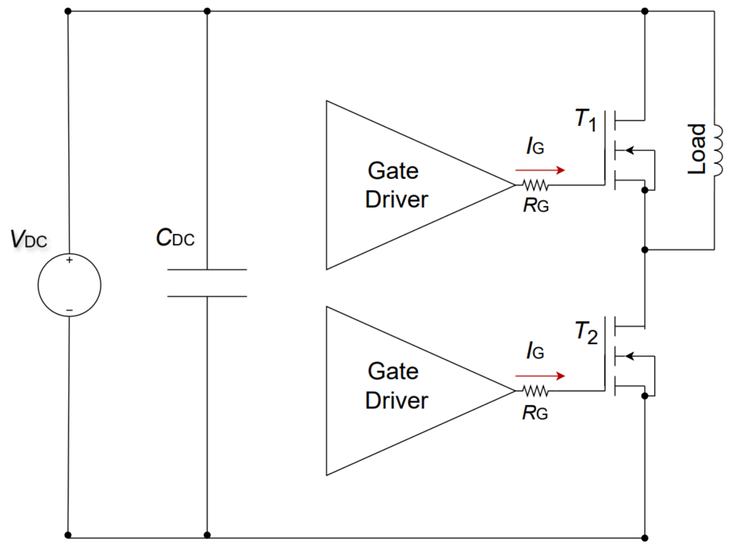
Comparative Analysis of Gate Driver Control Topologies: Effects on SiC MOSFET Switching Performance in Half-Bridge Configurations

Lan Fang, Venu gopal Mangali, Xin Jin, Fangbo Yin, Fangyuan Chen

Introduction

This work investigates the impact of voltage-controlled and current-controlled gate driver topologies on the switching behavior of power devices in half-bridge configurations.



Selecting the right gate driver plays a crucial role in controlling the slew rate of the drain-source voltage and drain-current to maximize the efficiency of SiC MOSFETs.

In this poster, three gate driver topologies were analyzed with respect to their impact on the switching characteristics of power devices under various operation conditions.

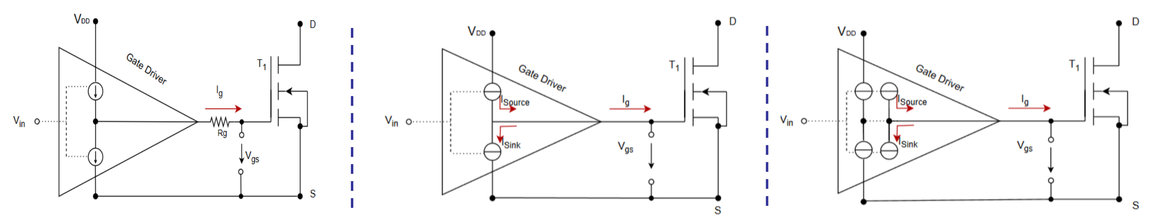
The results provide engineers and researchers with valuable options for enhancing the performance of power electronic systems.

Gate Driving Techniques:

Voltage Source Gate Driver (VSGD) ideally outputs a constant voltage V_{GS} to the gate of a power transistor.

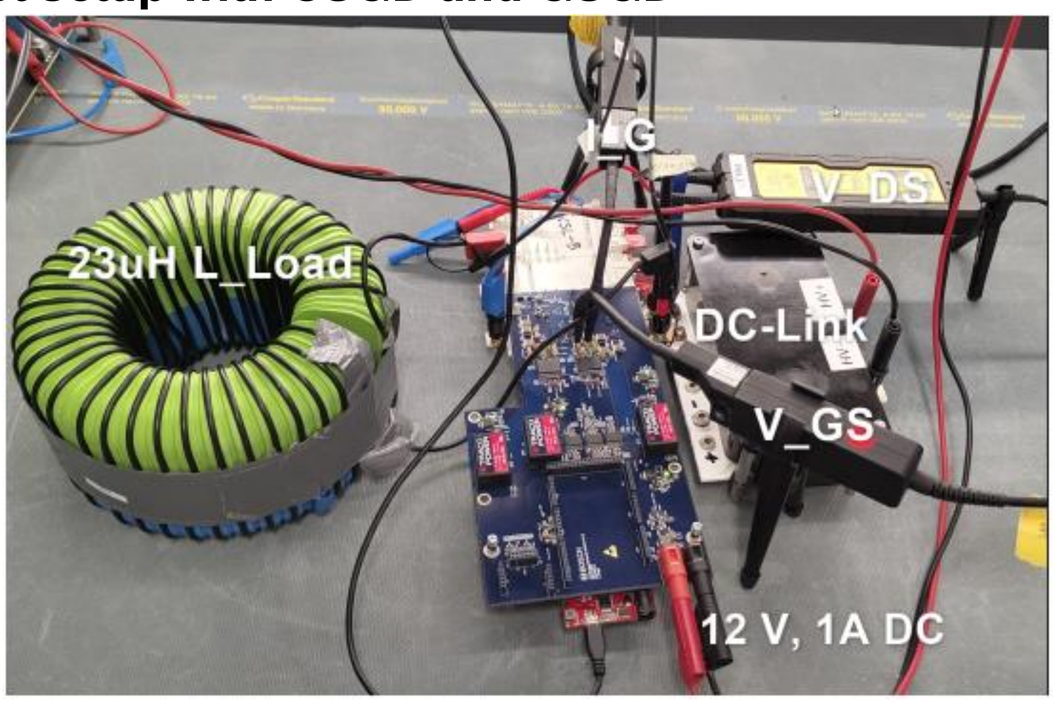
Current Source Gate Driver (CSGD) drives the gate with an ideal current, ensuring predictable charging and discharging speeds, and enabling precise control over the switching speed and transition time while maintaining robustness and reliability.

Gate Shaping Gate Driver (GSGD) differs from conventional CSGD by allowing the gate current (I_G) to be adjusted or programmed during different phases of the switching process.



Switching Characteristics

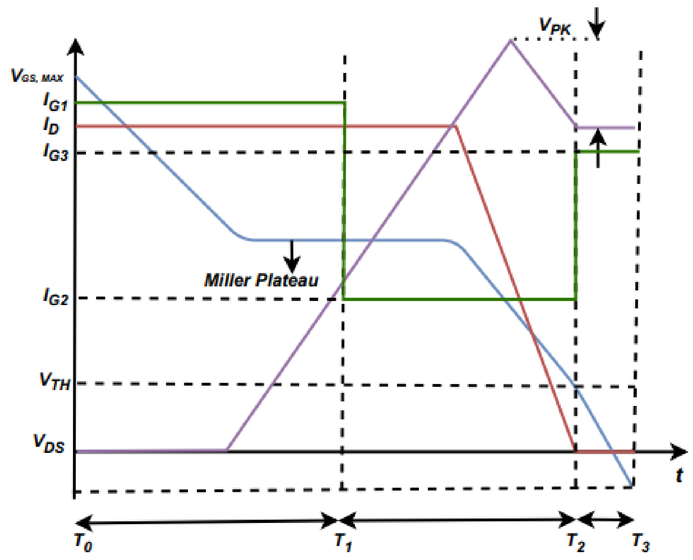
Test setup with CSGD and GSGD



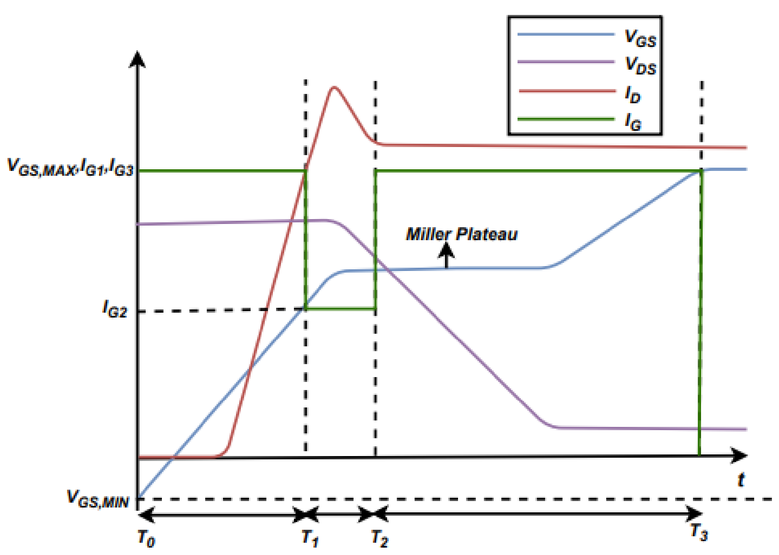
Gate profiles for T_{on} and T_{OFF}

I_{Load} (A)	$I_{\mathrm{G,ON}}$ (A)	$I_{\mathrm{G,OFF}}$ (A)
50	$1.5 \rightarrow 1 \rightarrow 1.5$	$1.2 \rightarrow 0.5 \rightarrow 1$
150	$1.5 \rightarrow 1 \rightarrow 1.5$	$1.2 \rightarrow 0.8 \rightarrow 1$
300	$1.5 \rightarrow 1 \rightarrow 1.5$	$1.2 \rightarrow 0.5 \rightarrow 1$
450	$1.5 \rightarrow 1 \rightarrow 1.5$	$1.2 \rightarrow 0.5 \rightarrow 1$
600	$2 \rightarrow 1 \rightarrow 2$	$1.5 \rightarrow 0.5 \rightarrow 1$

Gate shaping waveform for Turn-Off



Gate shaping waveform for Turn-On



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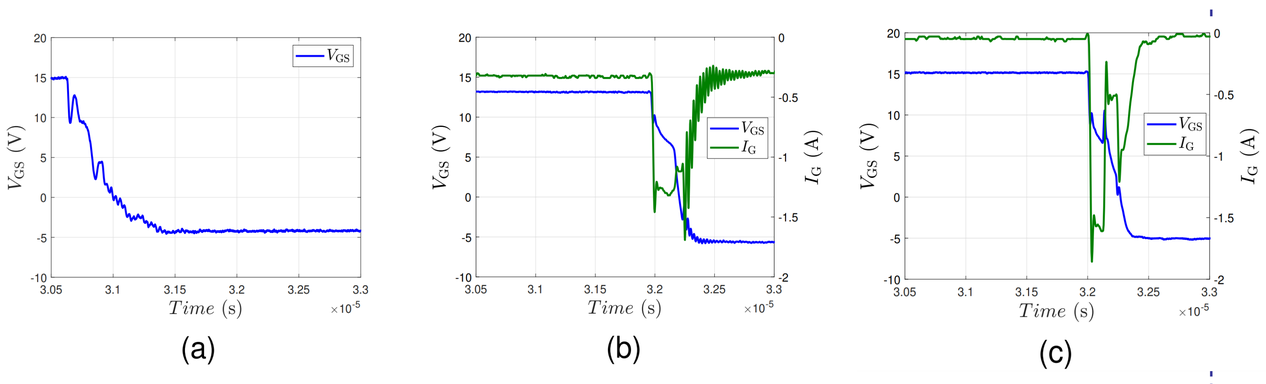
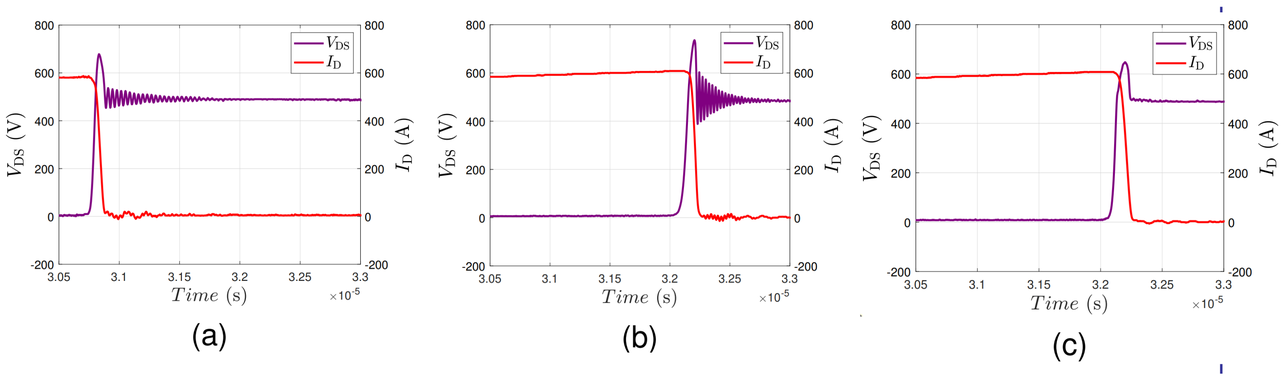
Comparative analysis of three topologies

Testing conditions V_{DS}= 550 V, I_D= 600A a) **VSGD**, b) **CSGD**, C) **GSGD**

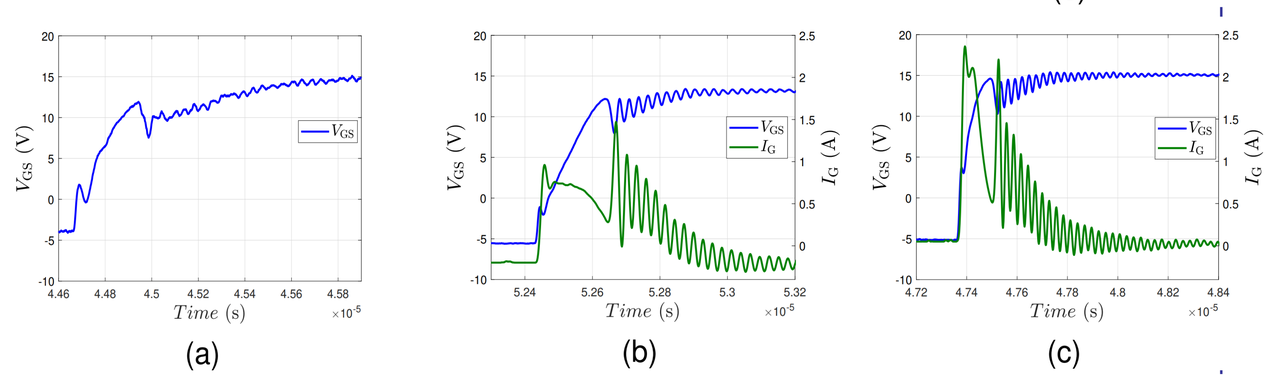
- Turn-off
- Gate-Source voltage
- Gate current



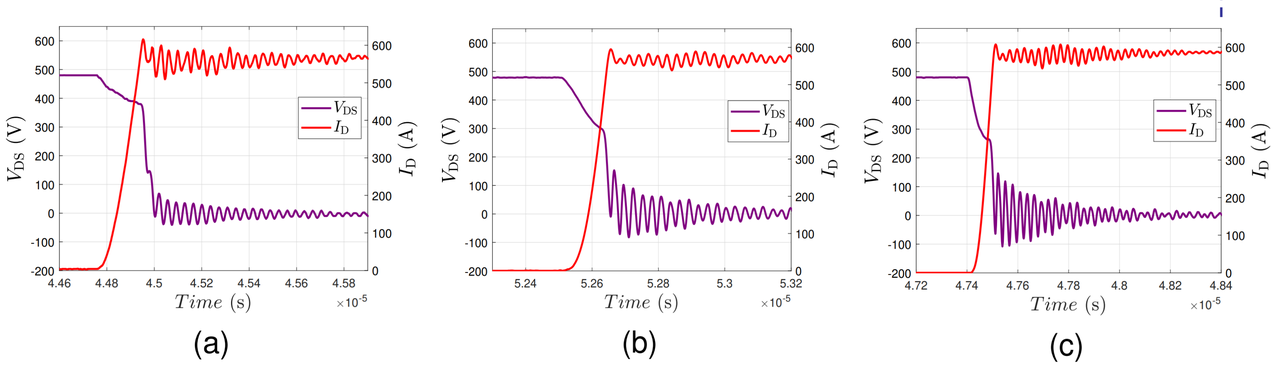
- Turn-off
- Drain-source voltage
- Drain current



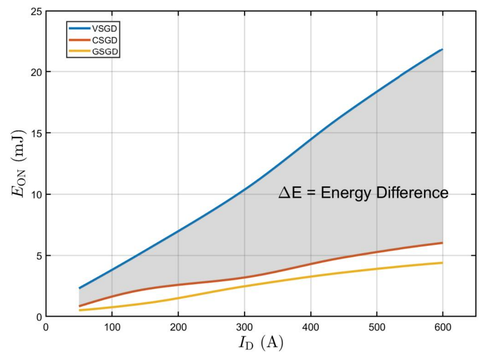
- Turn-on
- Gate-Source voltage
- Gate current



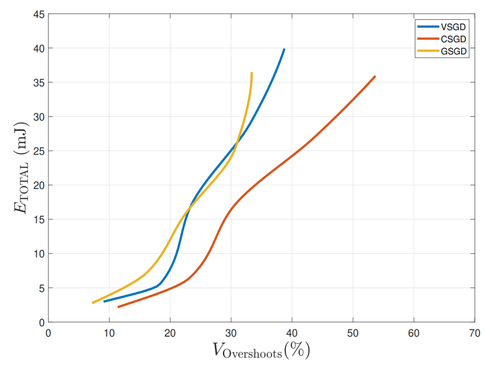
- Turn-on
- Drain-source voltage
- Drain current



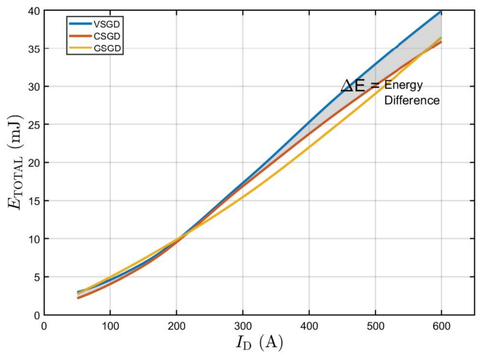
Drain current vs. Turn-on energy



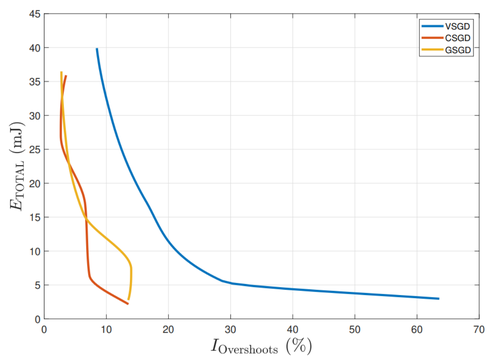
Voltage overshoots (%) vs. Total enengy



Drain current vs. Total energy

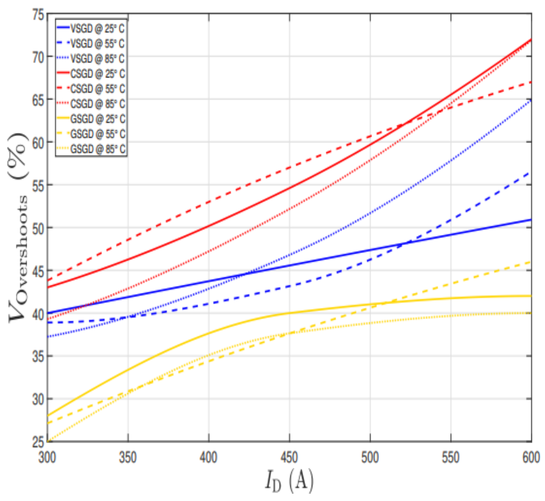


Current overshoots vs. Total energy

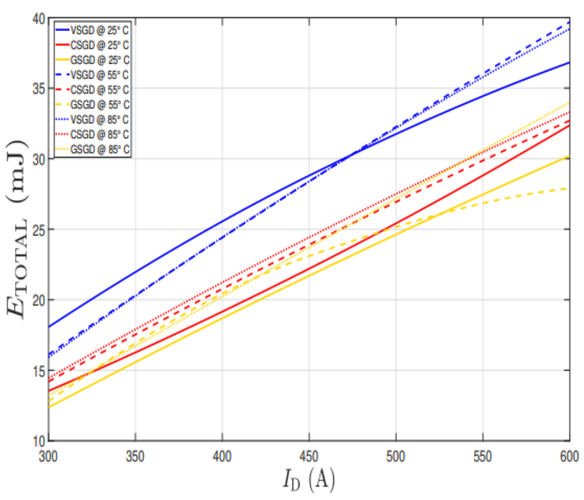


Performance comparison at increased temperatures

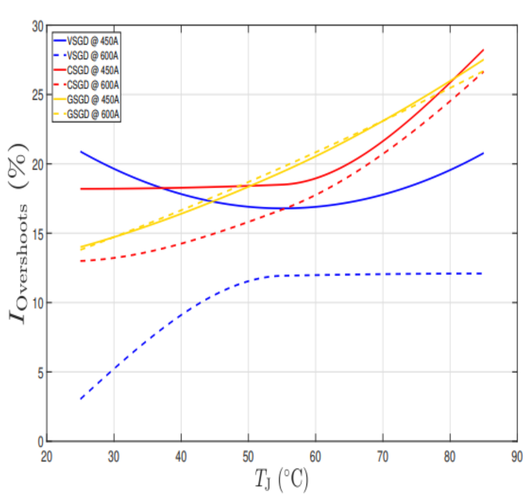
Voltage overshoots (%) Vs. Drain current



Turn-on energy vs. Drain current



Current overshoots (%) vs. Junction temperature



Conclusion

- The comparative evaluation of gate driver topologies under uniform conditions (550V DC, 50-600A load) through double-pulse testing highlights key differences in switching performance.
- Current source gate drivers effectively **reduce energy losses and overshoots**, offering improved performance during turn-on and turn-off behavior.
- Gate shaping-based current source drivers **dynamically adjust gate current**, reducing voltage overshoots and energy losses beyond the limits of conventional VSGD and CSGD.
- Research results demonstrate that precise switching control enables **saft operation** of SiC MOSFET half-bridges.