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ASIA SHANGHAI

Enhanced 900 A 1700 V ED Module with Micropattern Trench IGBT for High Performance and Reliability

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Introduction and motivation

- ED type modules are a staple of the power electronics industry
- Widely used in industrial drives, renewable energy and automotive applications
- Highly scaled and standard footprint -> large focus on economical value

Main design focus:

→ Provide best possible $/A performance

→ Rugged, low loss chipset

→ Suitable for a wide variety of applications

Module design

Summary

Main focus: improve module while reducing cost

→ Improve current carrying capability

→ Enhance power & thermal cycling reliability

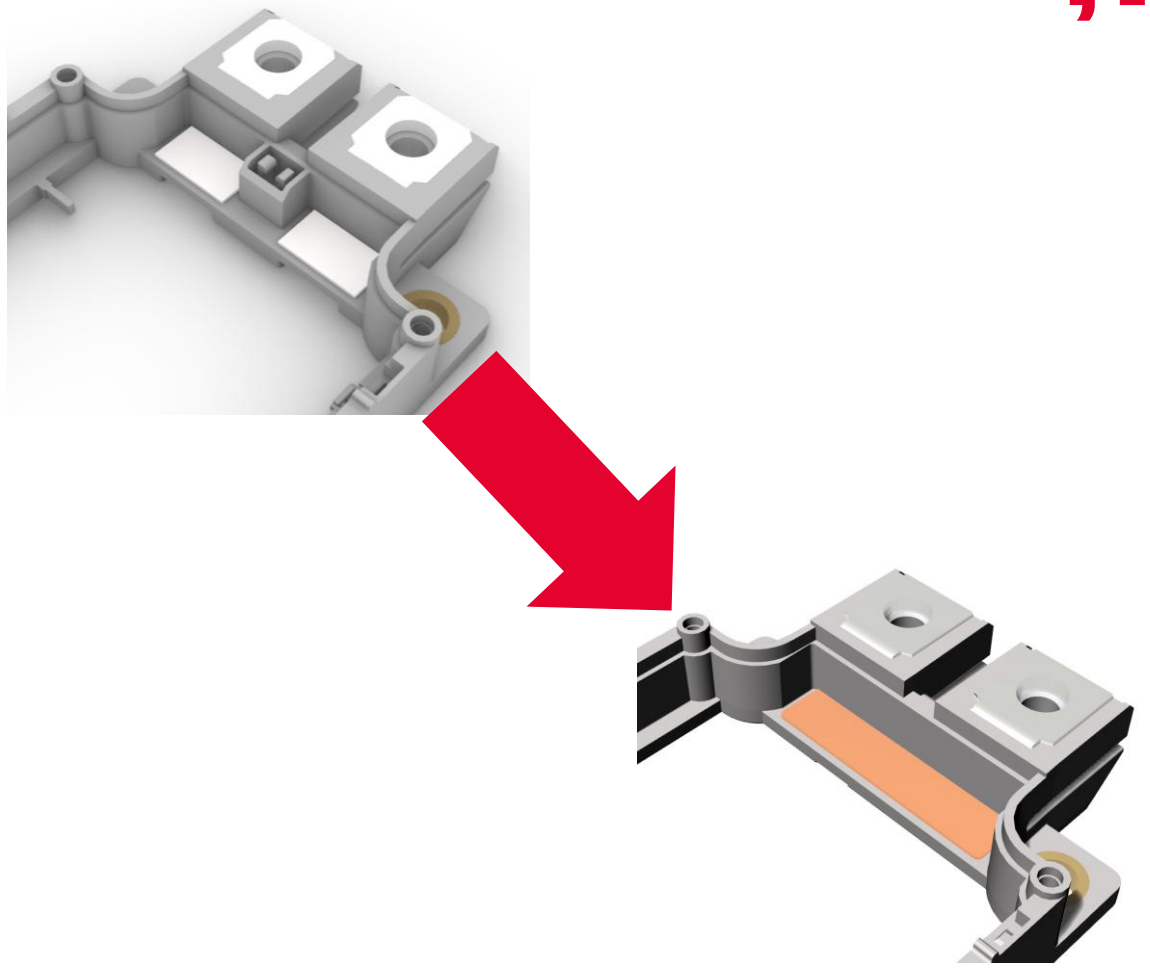
→ Reduce coupling on the IGBT for improved switching

→ Enable more chip area for higher power density

Module design

Improved current carrying capability

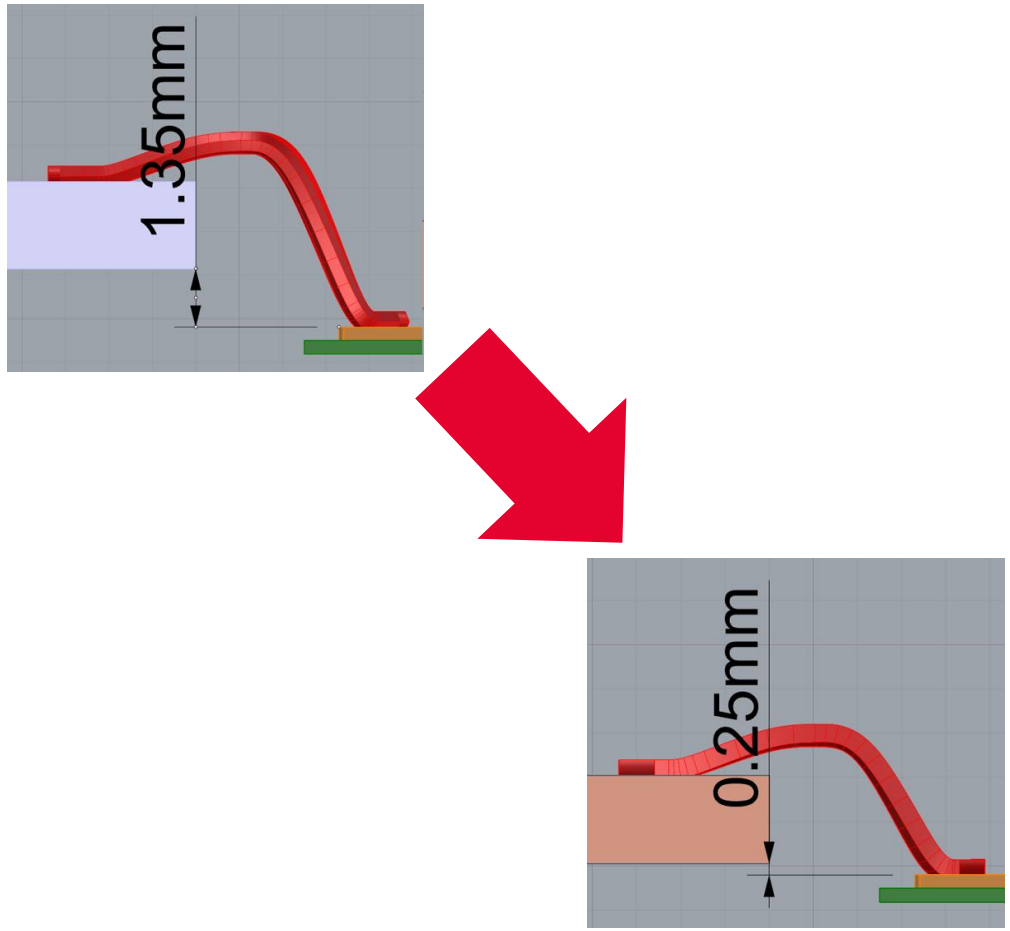
- Optimized power terminals for more bondable area
- Bare copper metallization for more stable bonding



Module design

Improved current carrying capability

- Optimized power terminals for more bondable area
- Bare copper metallization for more stable bonding
- 20mil copper wires & shorter loops on the terminals



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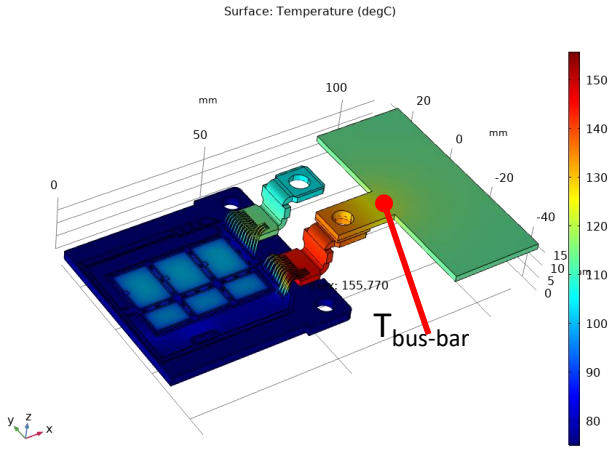
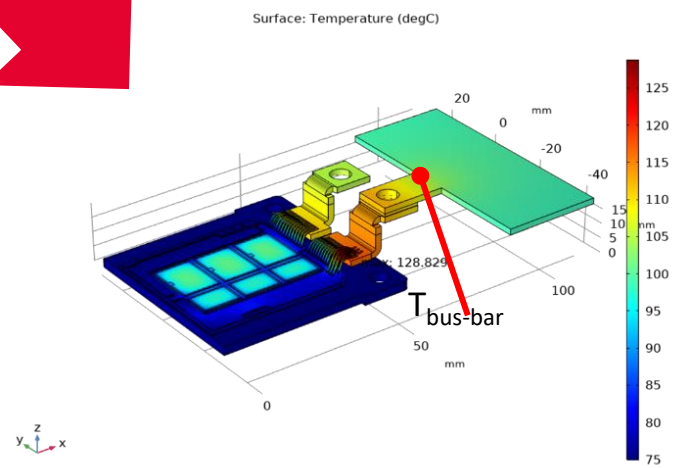


➔ The improvements lead to an average reduction in terminal temperature of more than 30 %



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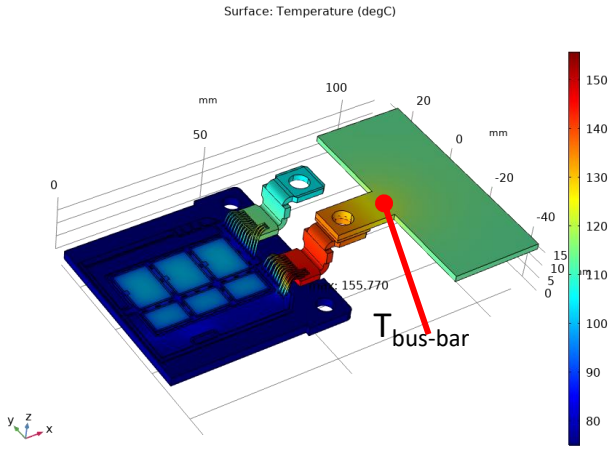

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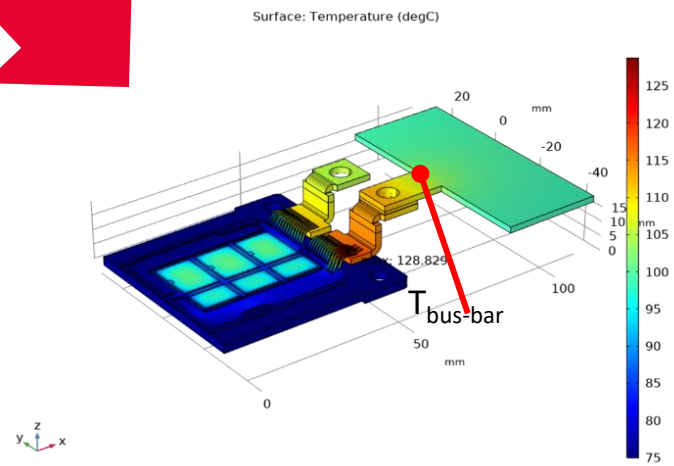
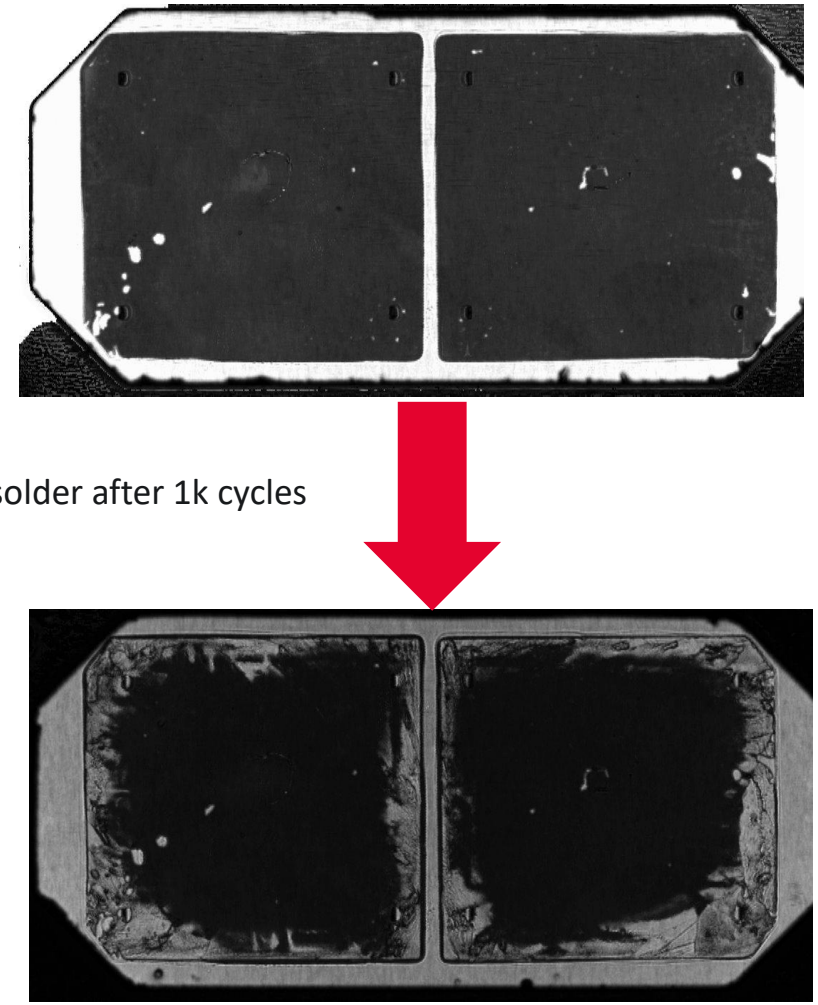
Terminal type	750 A Design (K)	900 A Design (K)	Delta (K)	Delta (%)
DC+	72.2	50.9	21.3	**29.5**
DC-	82.4	52.9	29.5	**35.8**
AC	61	44	17	**27.9**



Module design

Enhanced thermal cycling reliability

- The soldering is improved for both the die attach and the substrate to baseplate
- A novel solder material is used to greatly increase the reliability of the solder joints



Module design

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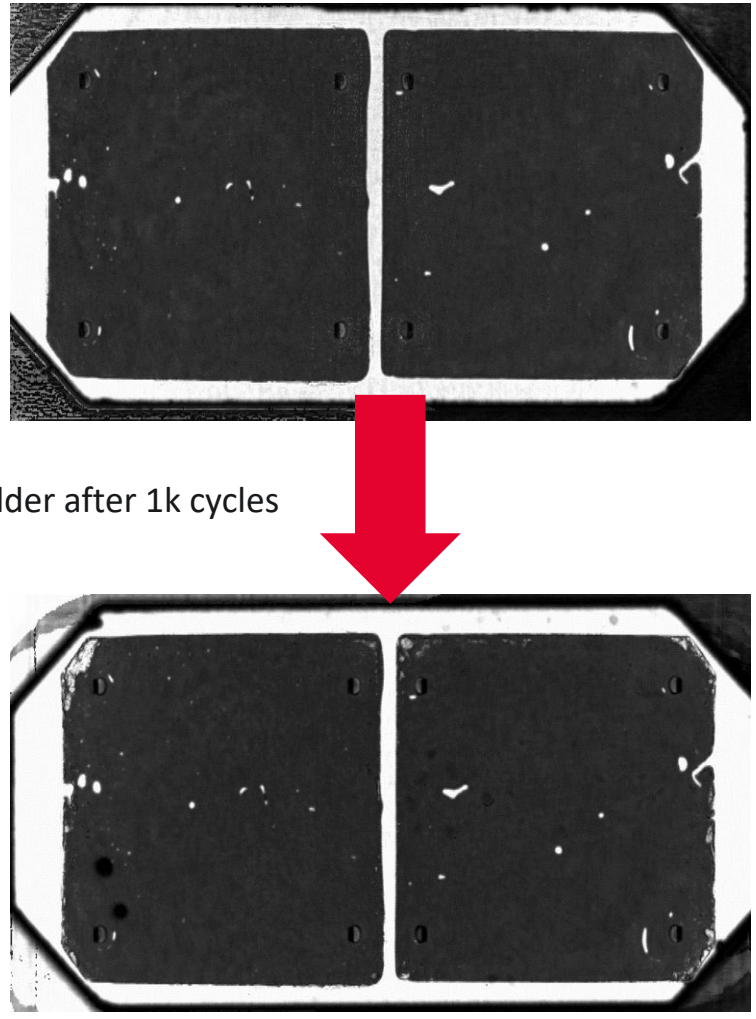
T_{min} = -40 °C, T_{max} = 125 °C, t_{change} = 3 s, t_{hold} = 30 min

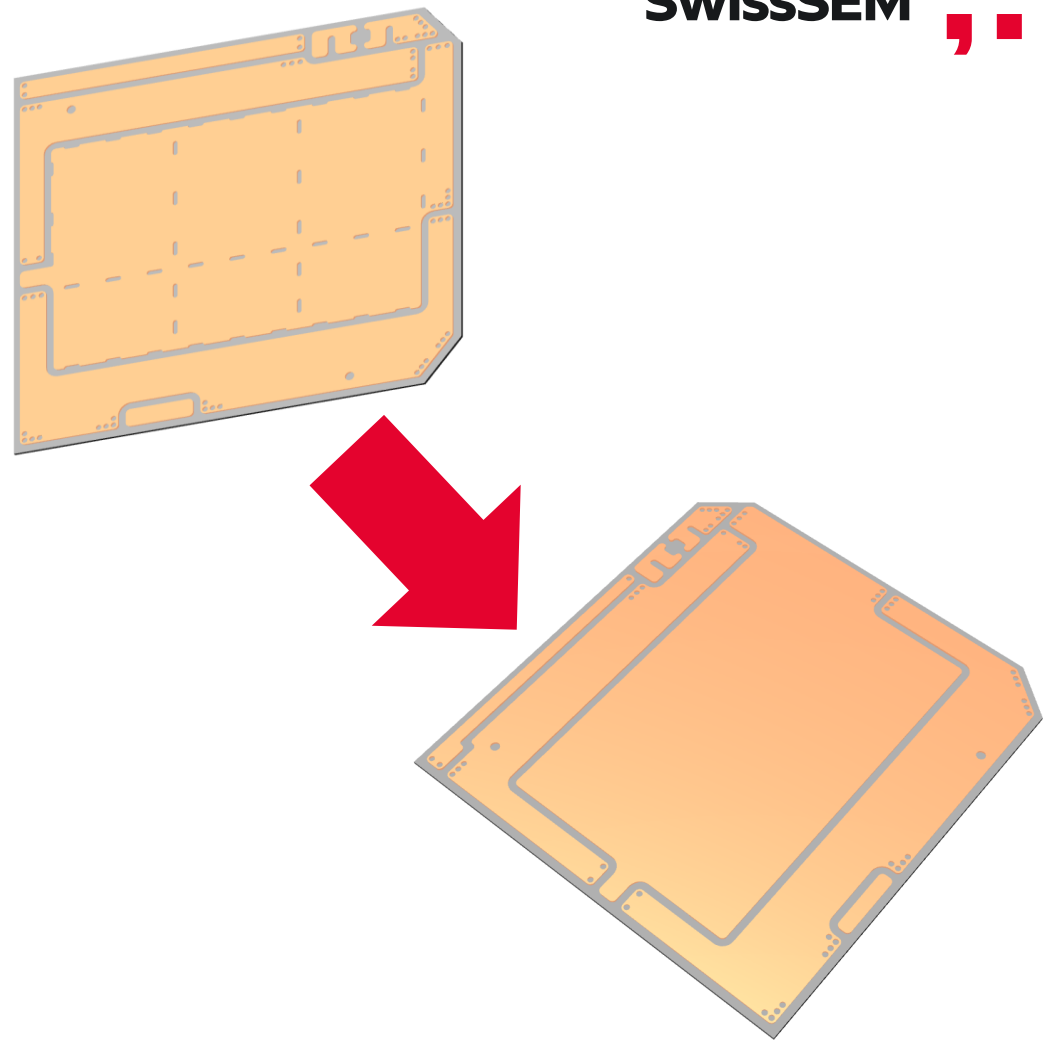


Improved solder after 1k cycles

Module design

Improved DBC substrate layout

- More chip area, more flexible chip placement

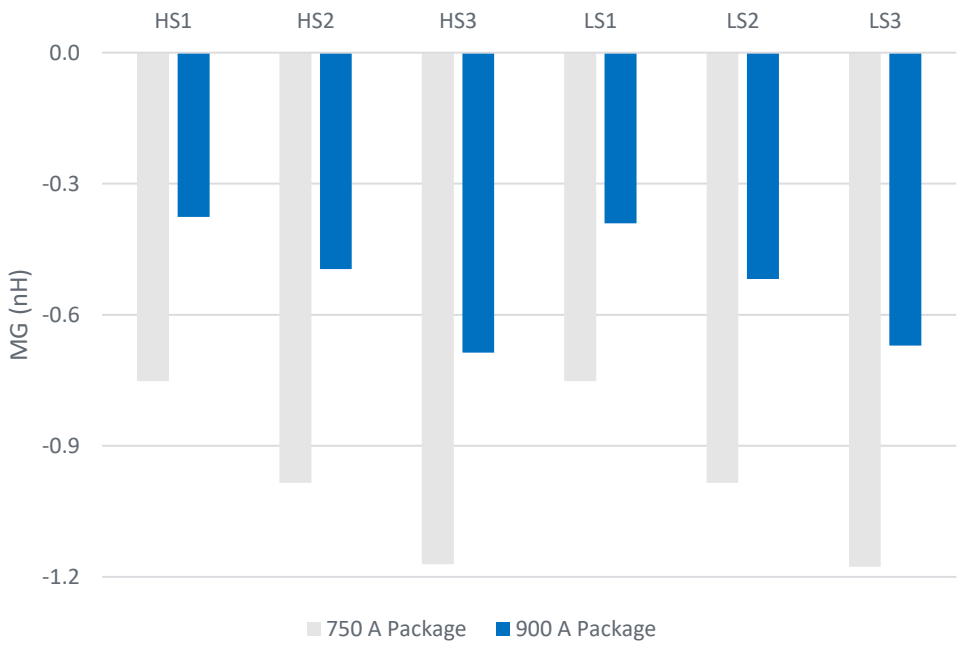


Module design

Improved DBC substrate layout

- More chip area, more flexible chip placement
- Reduced GE coupling for improved switching behavior

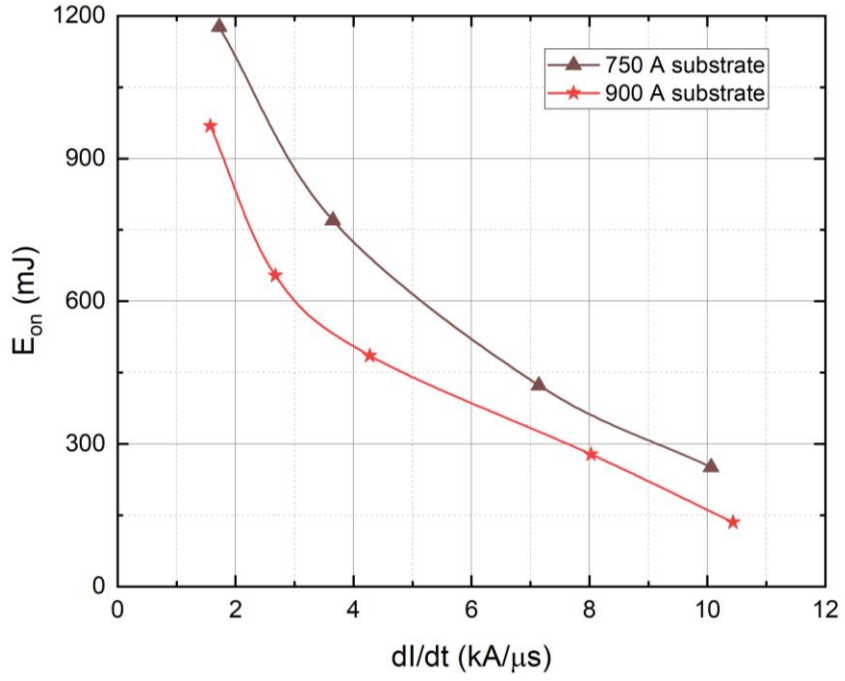
➔ GE coupling is reduced by 30 – 50 %

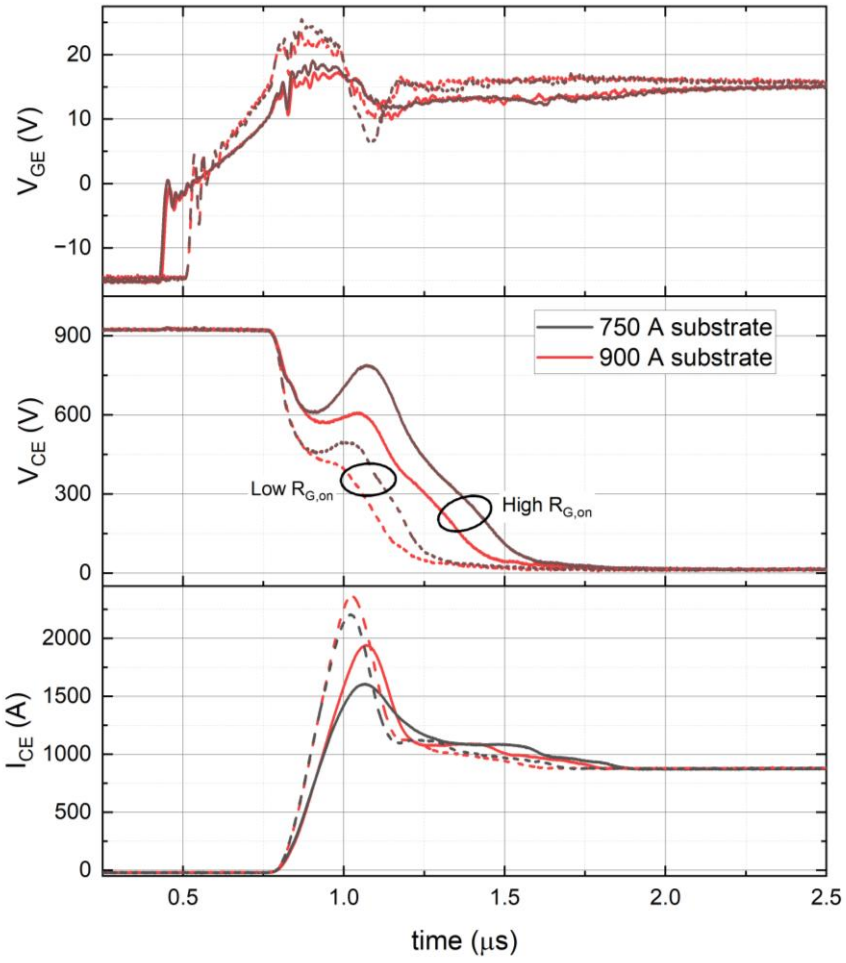


Module design

Improved DBC substrate layout

- More chip area, more flexible chip placement
- Reduced GE coupling for improved switching behavior
- Faster switching, reduced Eon





IGBT cell design

LC^3 IGBT

IGBT cell improvement drivers:

→ Higher cell density by feature size shrinking

→ Optimized arrangement of gate and emitter trenches

→ Carrier confinement

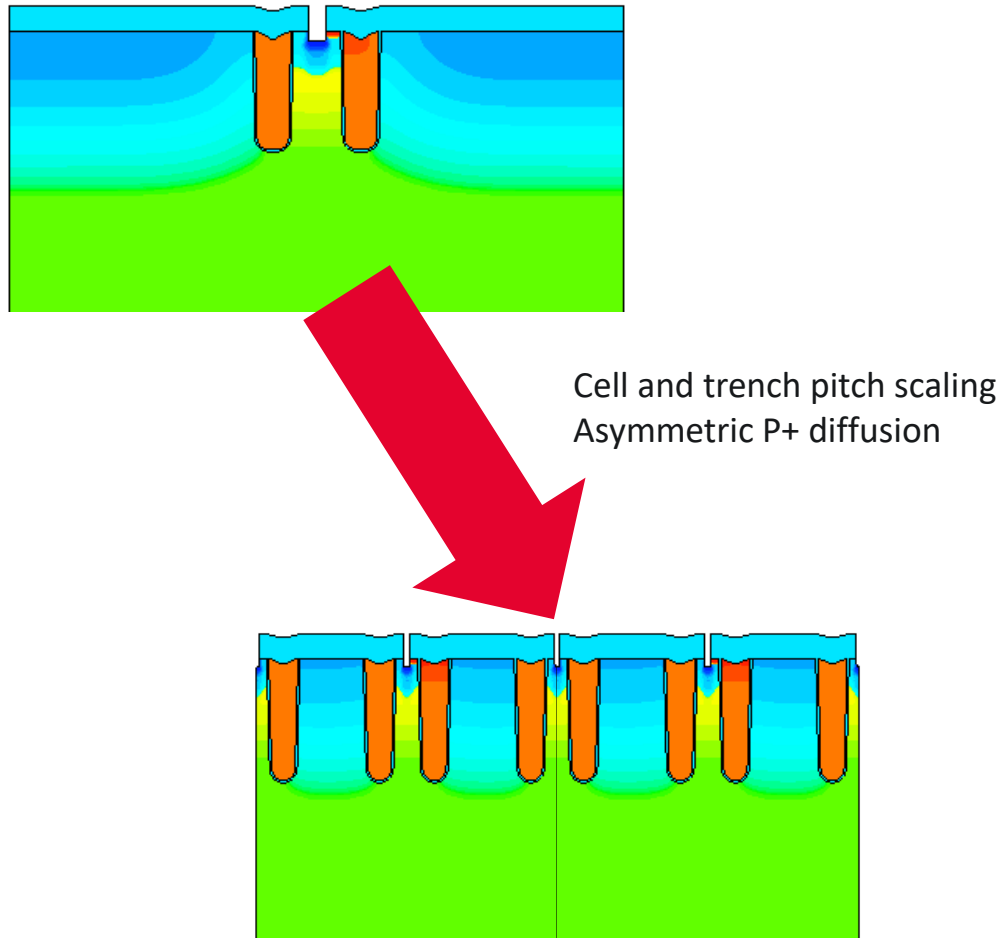
Conduction and switching losses can be improved, but we need to consider:

→ Turn-off controllability (Peak voltage at turn-off)

→ Reverse bias safe operating area (RBSOA)

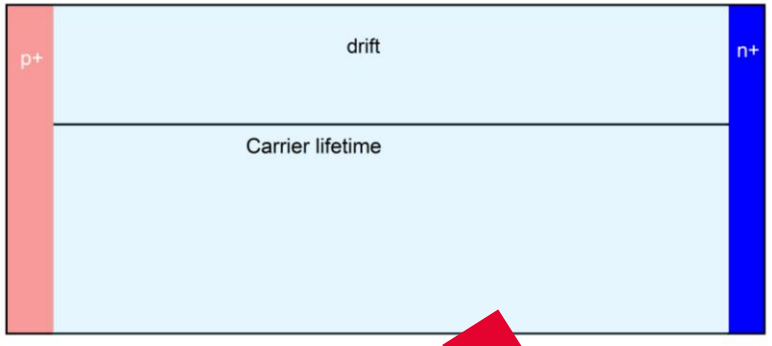
→ Short-circuit safe operating area (SCSOA)

➔ Micropattern trench IGBT with LC^3-concept allows further improvement on the technology curve while keeping controllability



Diode design

QLLC Diode



Diode improvement drivers:

→ Anode injection tuning

→ Carrier lifetime control

→ Drift region thickness

Higher anode efficiency
and carrier lifetime control

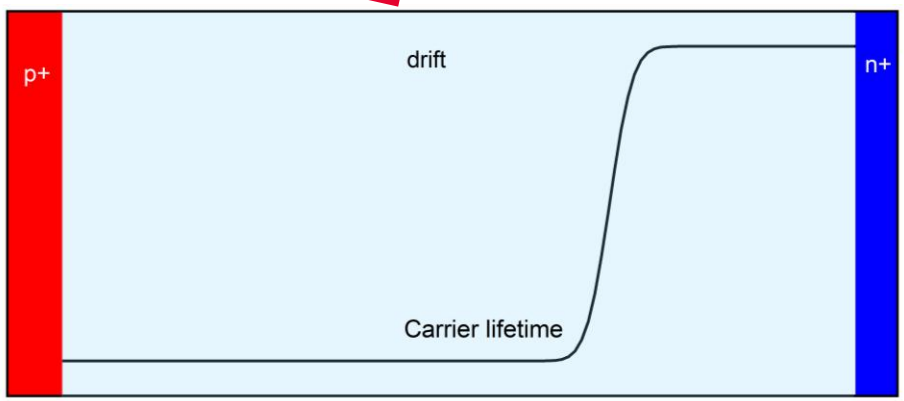
Conduction and switching losses can be improved, but we need to consider:

→ Soft recovery behavior

→ Diode safe operating area (DSOA)

→ Temperature coefficient

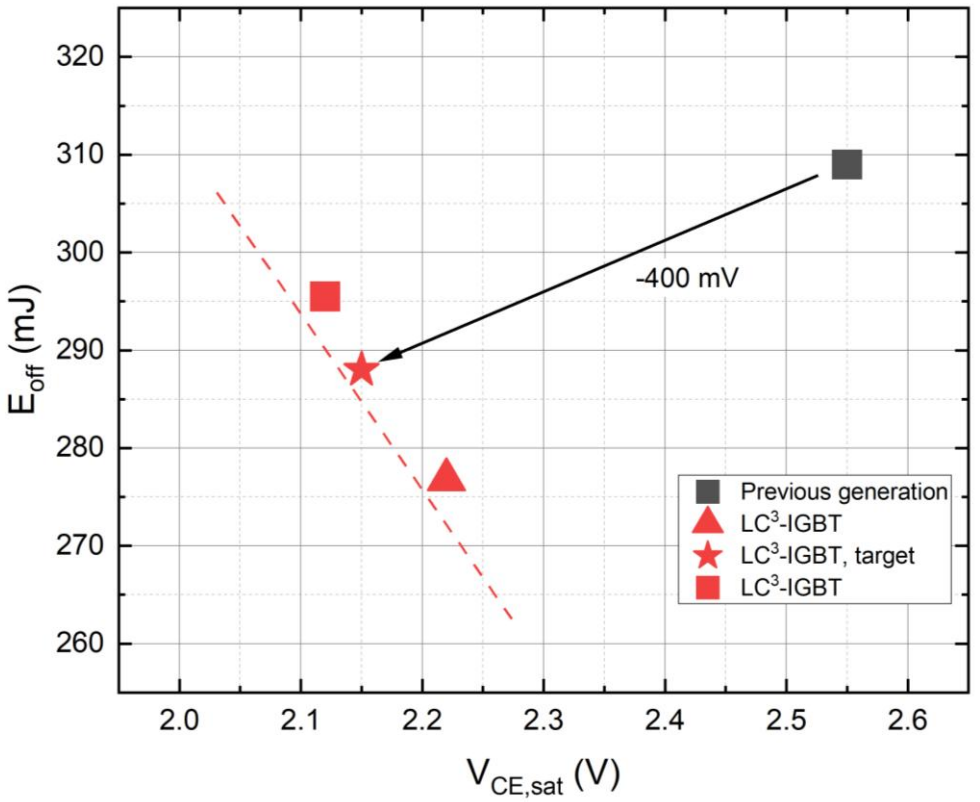
➔ Diode with novel QLLC technology allows for increased emitter dose and thinner drift region while keeping the soft recovery behavior



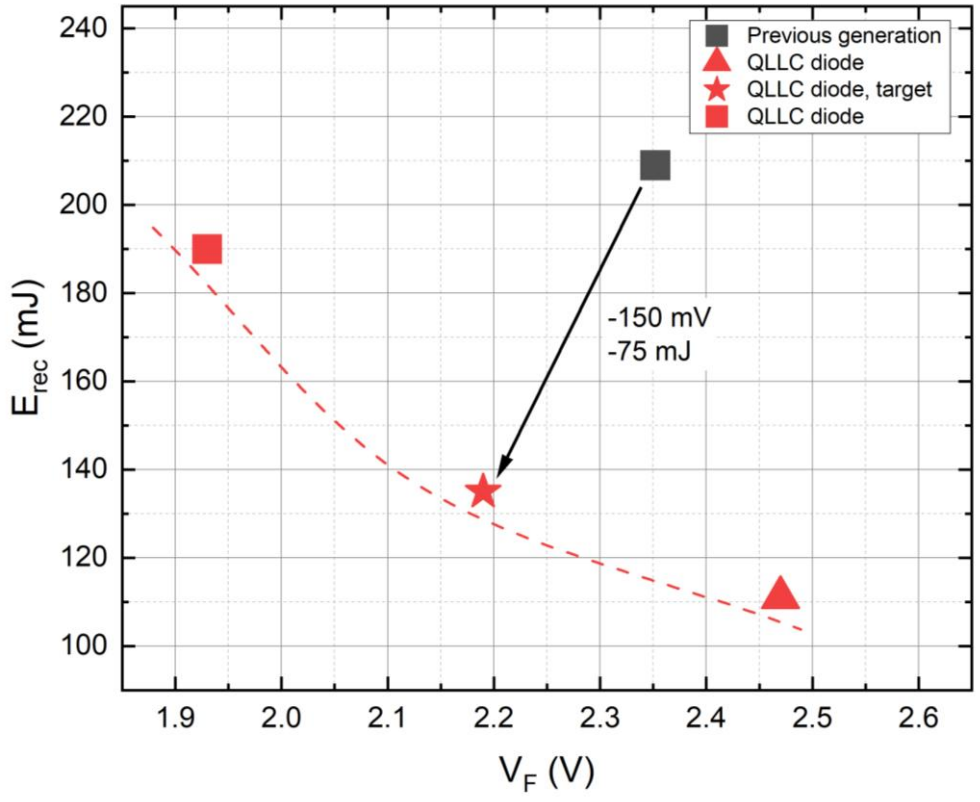
Technology curve

900 A, 900 V, L_σ = 35 nH, 175 °C

Technology curve IGBT ($R_{G,off}$ = 0.5 Ω)



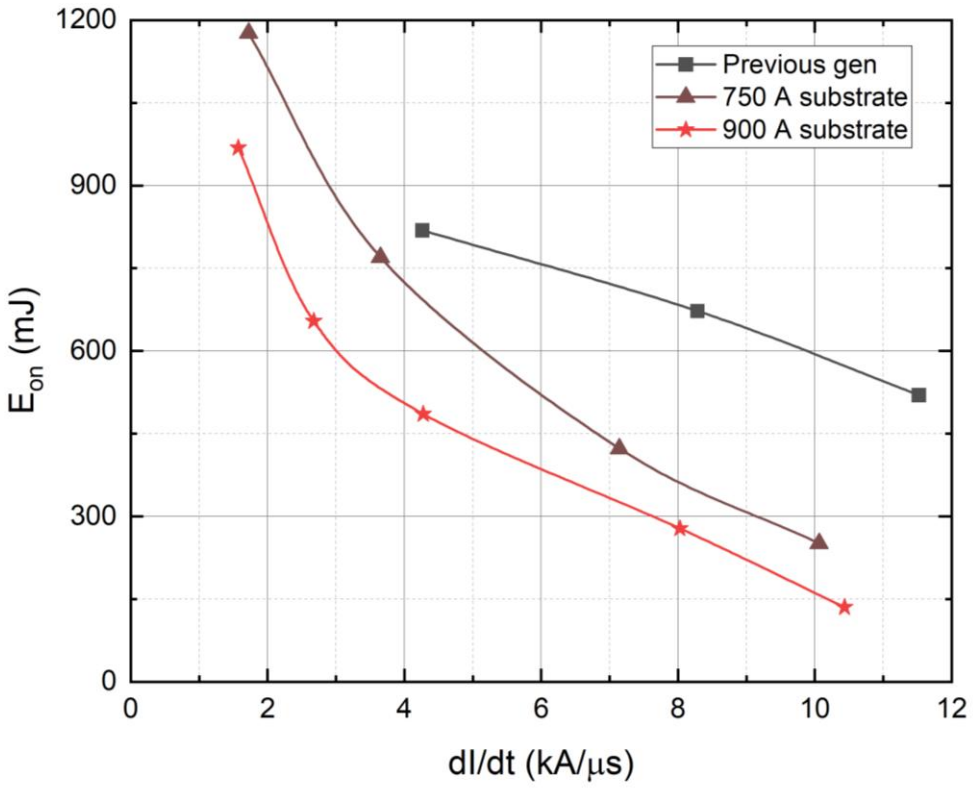
Technology curve Diode (dI/dt = 9 kA/µs)



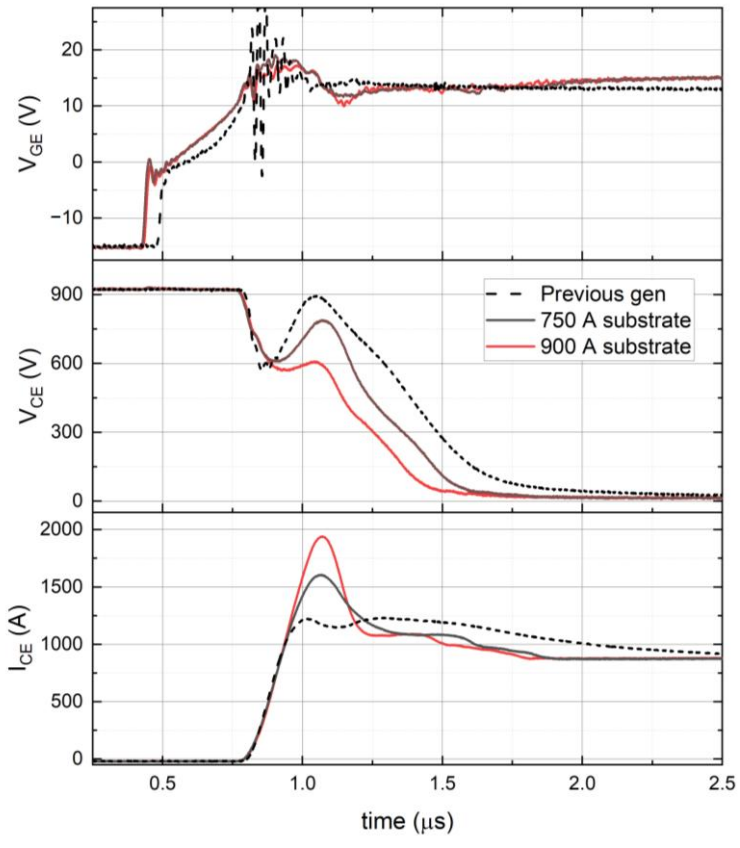
IGBT turn-on

900 A, 900 V, L_σ = 35 nH, 175 °C

Turn-on energy vs dI/dt



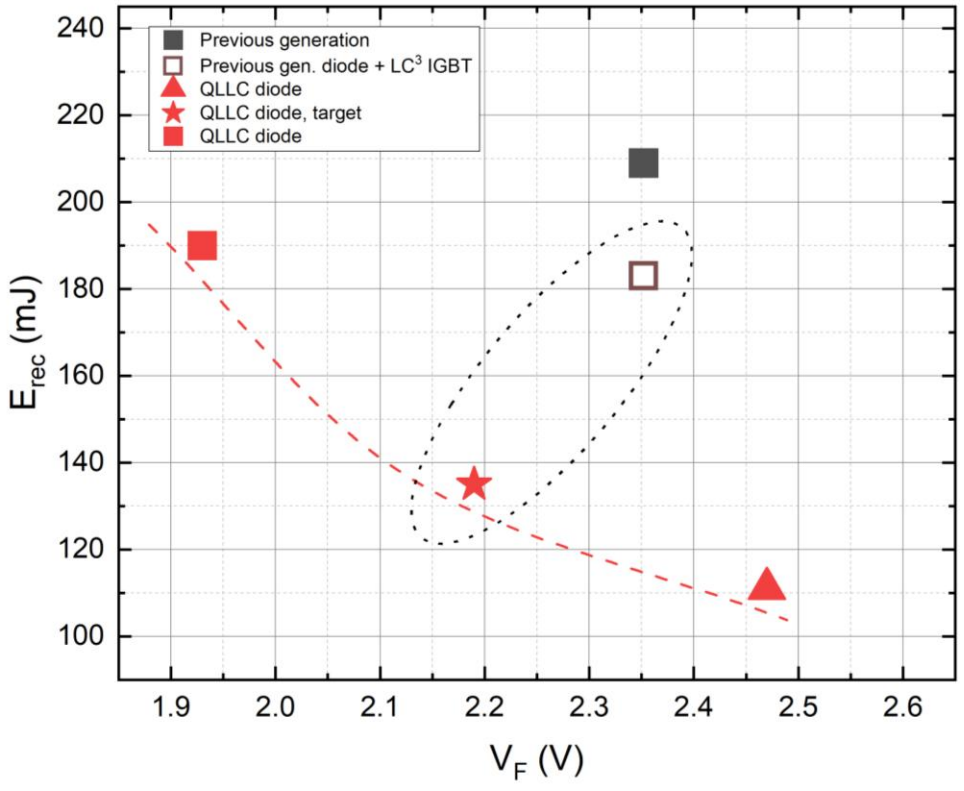
Turn-on waveform ($R_{G,on}$ = 0.5 Ω, 1.5 Ω for previous gen)



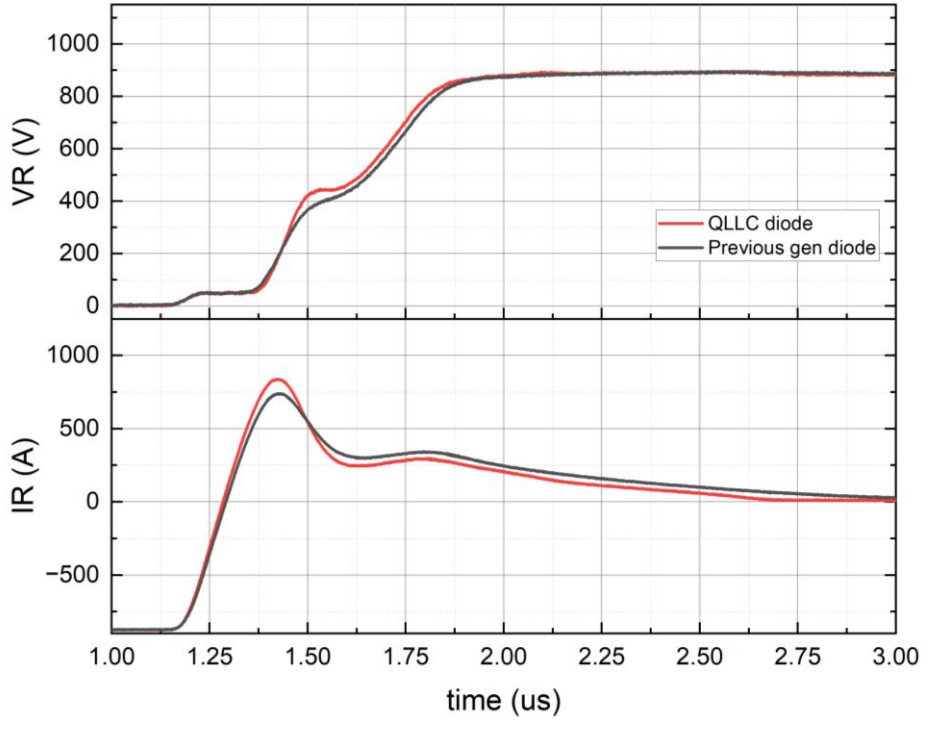
Diode recovery

900 A, 900 V, $R_{G,on}$ = 0.5 Ω, L_σ = 35 nH, 175 °C

Technology curve diode (both diodes with new IGBT)



Recovery waveform ($R_{G,on}$ = 0.5 Ω)

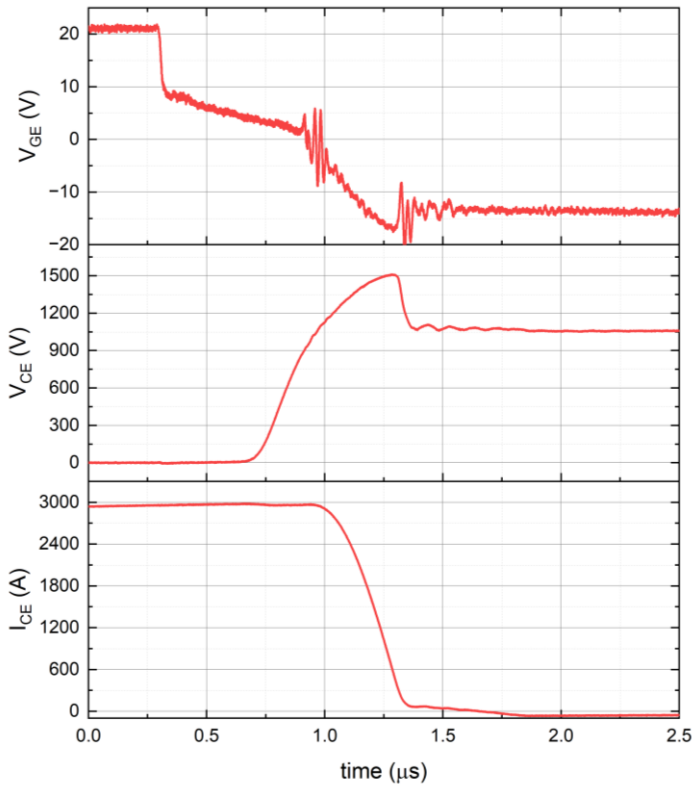


Safe operating area

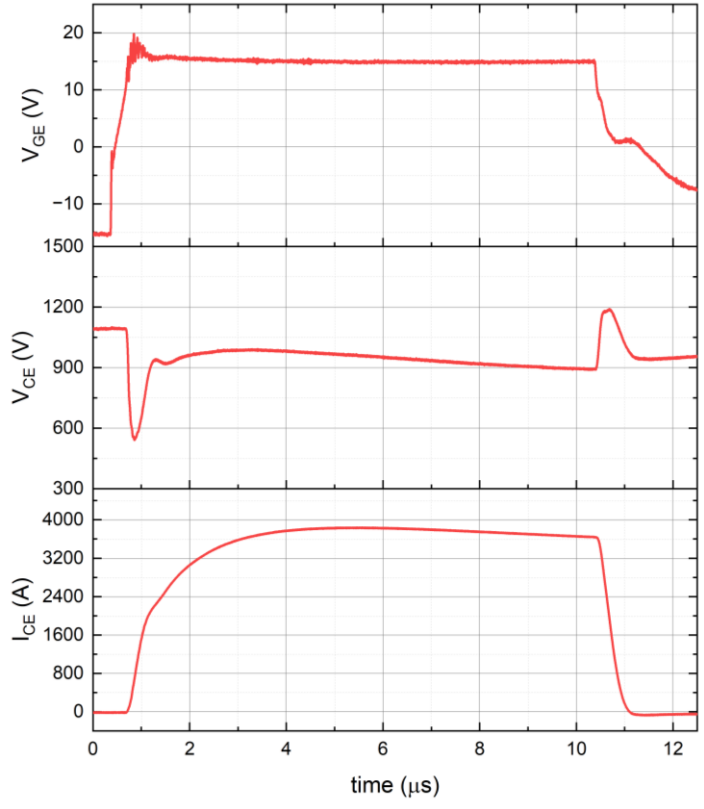
RBSOA / SCSOA L_σ = 35 nH, 175 °C

- The novel LC³ IGBT is extremely robust in both RBSOA and SCSOA
- Large margin in SOA improves yield and reduces risk of failures in the field

RBSOA, 1100 V, 3000 A



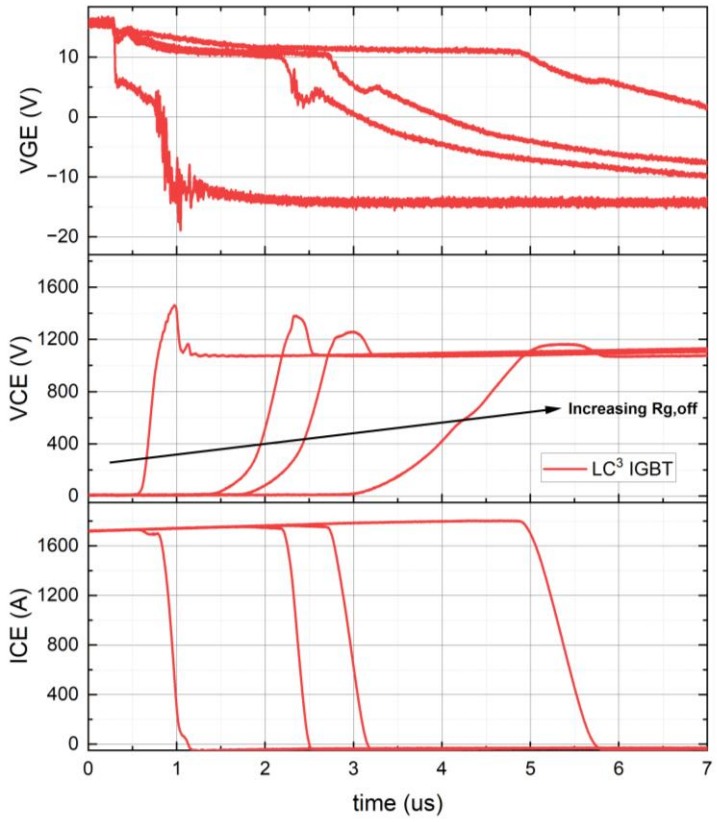
SCSOA, 1100 V, 10 µs



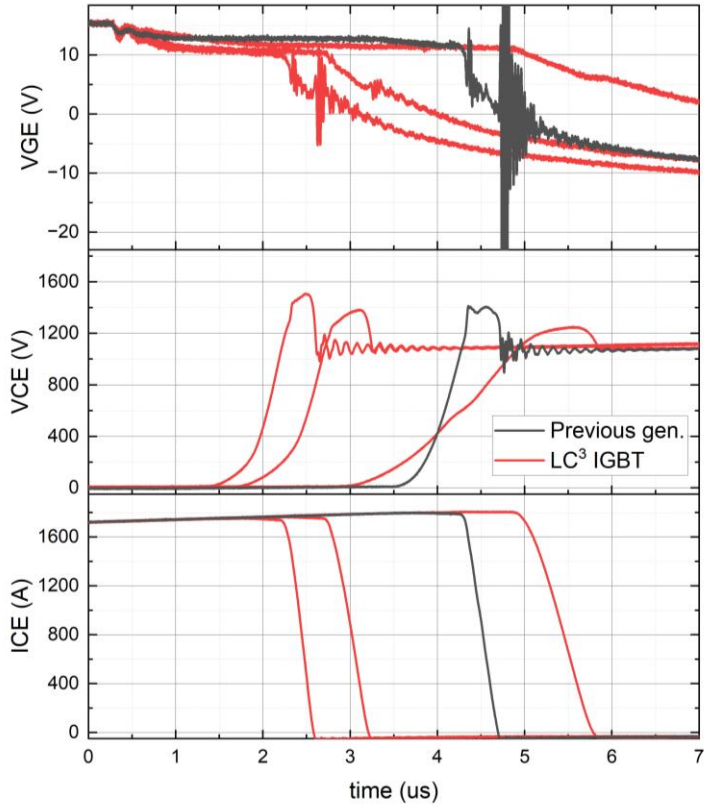
Turn-off controllability waveforms

I_{CE} = 1800 A, V_{CC} = 1100 V, $R_{G,off}$ = 0.5 … 40 Ω, 25 °C

L_σ = 35 nH



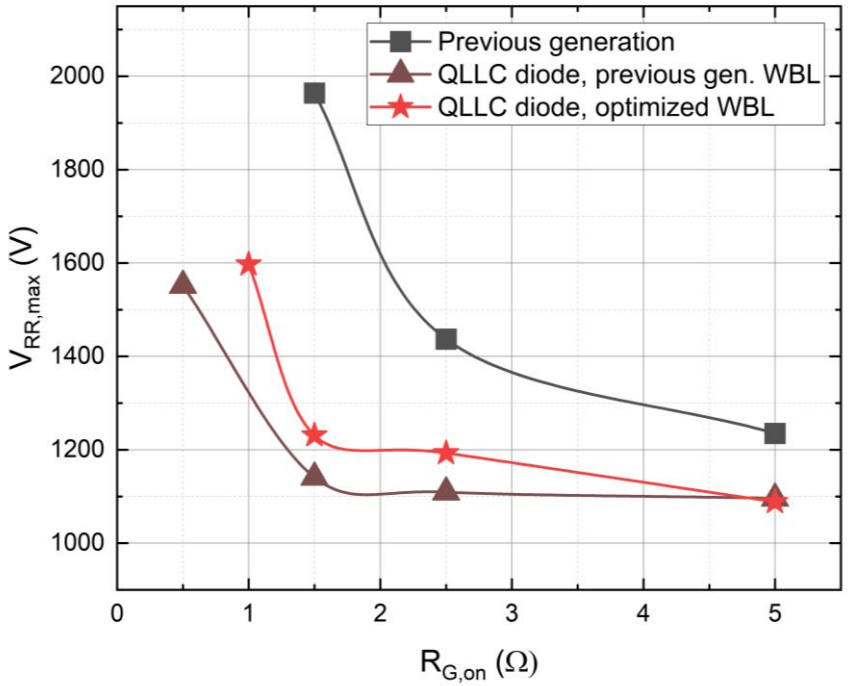
L_σ = 95 nH



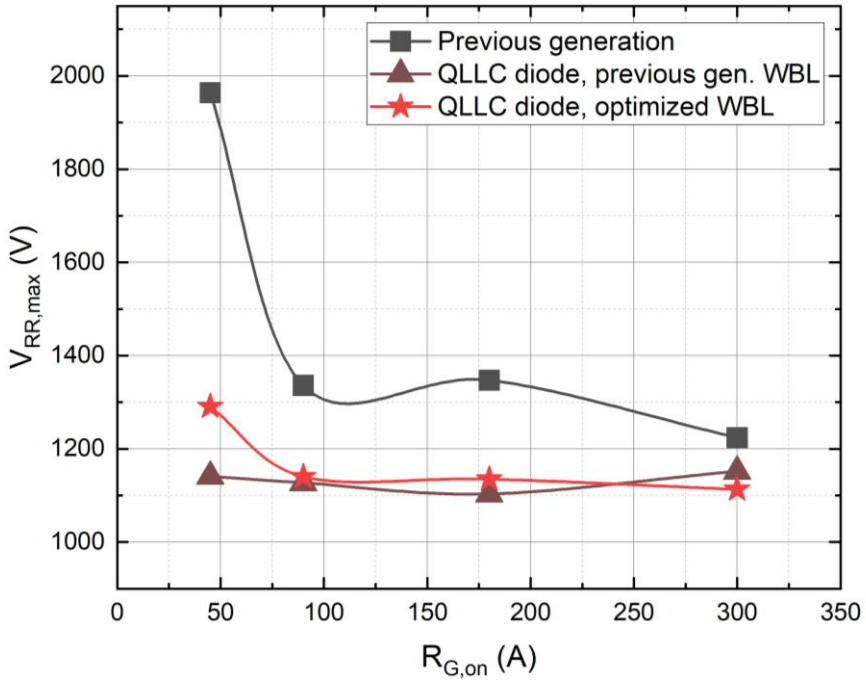
Diode softness

1100 V, I_F = 45A, L_σ = 95 nH, 25 °C

Peak recovery voltage vs $R_{G,on}$



Diode softness waveforms, I_F = 45 A, $R_{G,on}$ = 1.5 Ω



→ Improved diode shows significantly improved softness and lower losses at the same time

Summary and conclusion

- Summary:
  - The enhanced 900 A ED packaging from SwissSEM Technologies has been introduced
  - The new module features improved power terminal design, optimized bond-wire layout and DBC design, as well as a more reliable solder material
  - A new 1.7 kV 900 A chipset has been developed and the results shown
- Conclusion:
  - The new SwissSEM 900 A ED module features higher current carrying capability, better thermal cycling performance and enables faster switching
  - The novel chipset features class leading losses and SOA ruggedness
  - Inquire at our booth (N5 C01) for sample availability
  - Check our website for detailed product information: https://www.swiss-sem.com/product-catalogue

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6 – 8.5.2025
NUREMBERG, GERMANY

Thank you for the attention!

I‘m pleased to answer your questions.

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Messe Frankfurt Group