pcim ASIA SHANGHAI

400 V SiC MOSFET Unlocks New Efficiency and Power Density Ranges for Server and AI Power Supply Solutions

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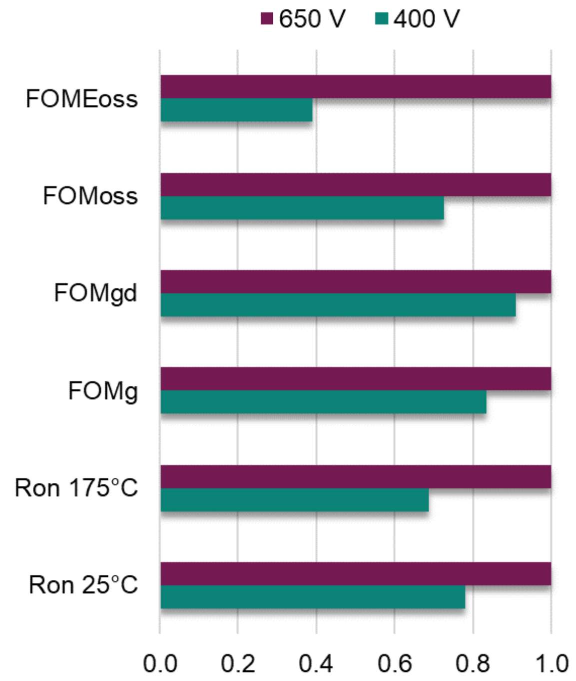
Presentation Outline

400 V CoolSiC™ MOSFET Properties and Benefits

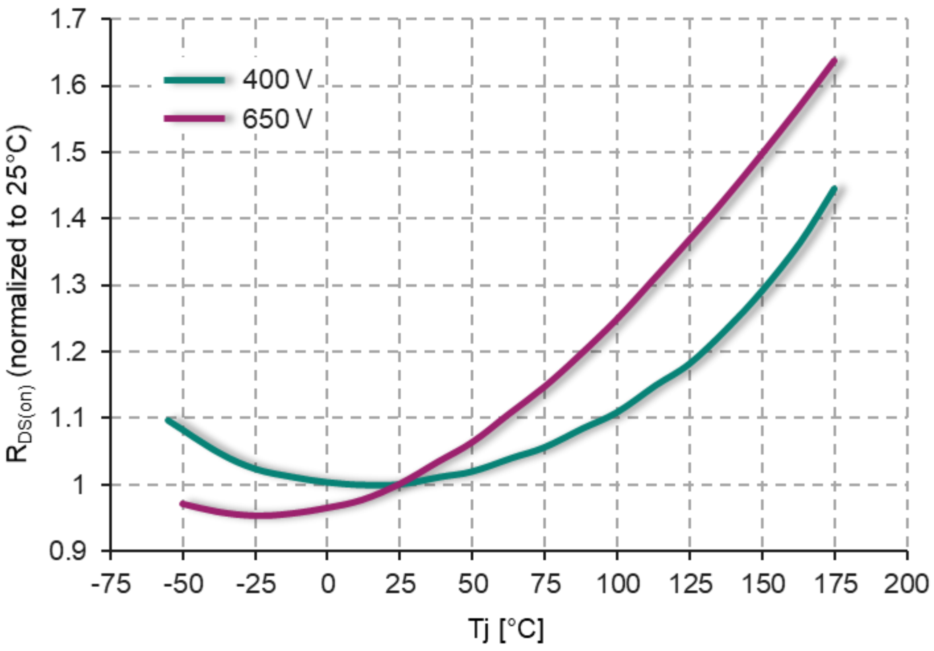
400 V CoolSiC™ G2 MOSFET

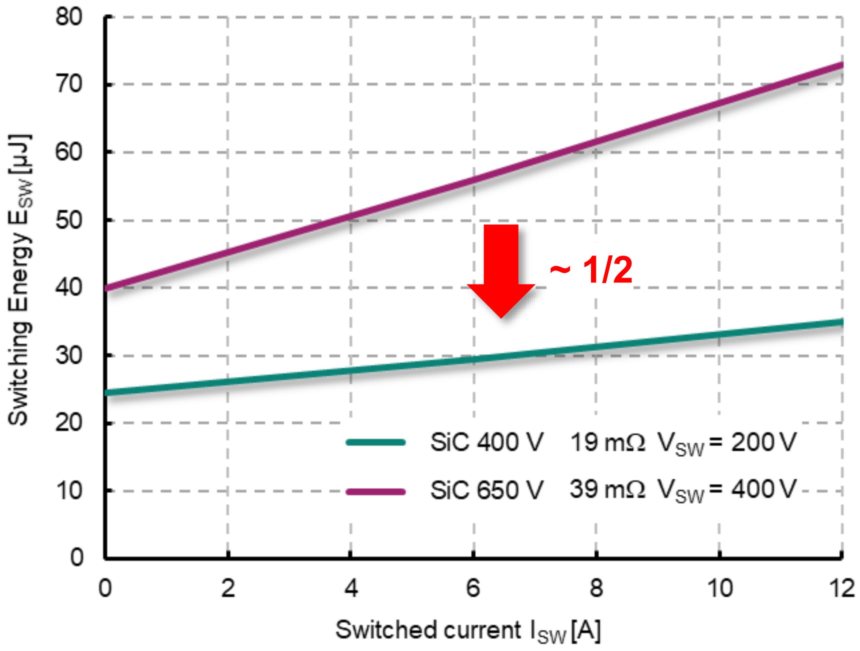
Device properties on a glance

- CoolSiC G2 400 V provides excellent FoM improvements compared to the 650 V reference
- the on-resistance of the 400 V device increases only by 11% with temperature rise from 25°C to 100°C
- 400 V device shows clearly lower switching losses even at half the on-resistance



FOMs defined at V_{DS} = 200 V for 400 V SiC and at V_{DS} = 400 V for 650 V SiC reference part





400 V CoolSiC™ G2 MOSFET

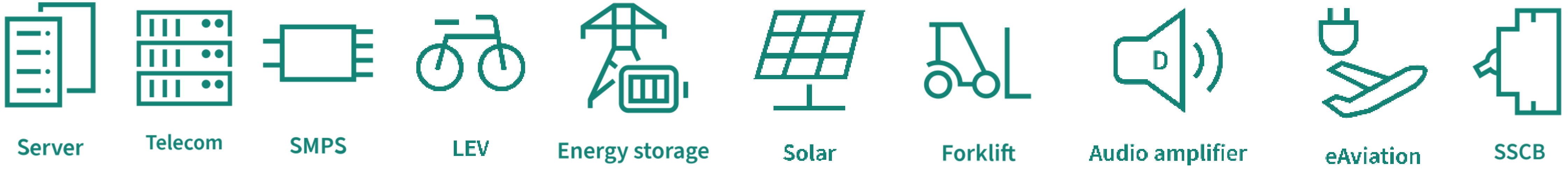
Opportunities where 400 $V_{(BR)DSS}$ fits perfectly

Unique opportunity to address applications with high performance MOSFETs with $V_{(BR)DSS}$ between 200 V and 650 V

V_{BUS}

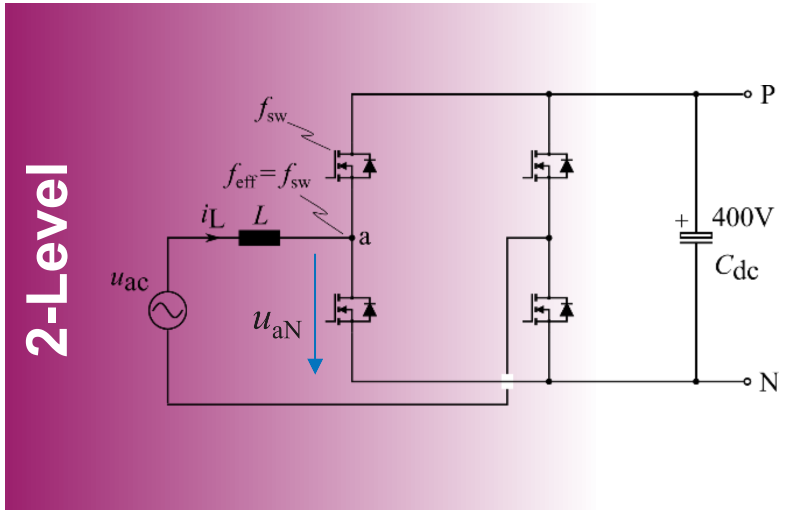
≤ 300 V 2-level topology

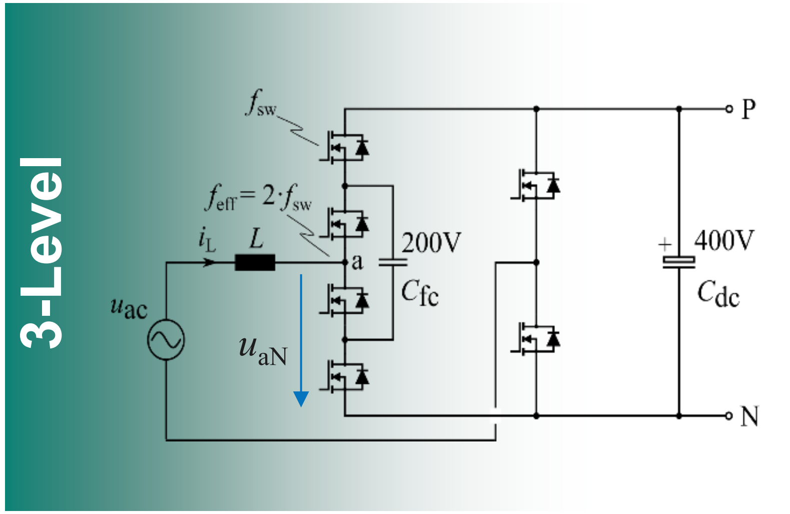
≤ 600 V 3-level topology



3-Level Flying Capacitor PFC vs. 2-Level Totem-Pole PFC

3-Level Trade-Offs … power density vs. losses

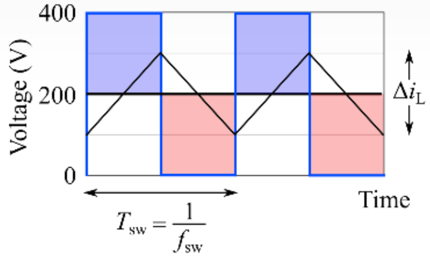




Case 1: $f_{sw}(3L) = f_{sw}(2L)$

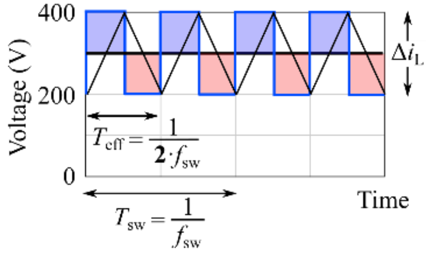
- identical losses of semiconductors
- much smaller L and EMI filter

$$P_{cond} = I_{rms}^2 \mathbf{R_{on}}$$
$$P_{sw} = f_{sw} \mathbf{E_{sw}}$$



4x smaller

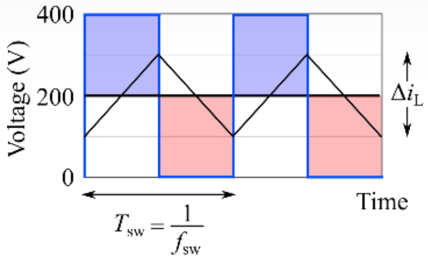
$$P_{cond} = \cancel{2} \cdot I_{rms}^2 \frac{\mathbf{R_{on}}}{\cancel{2}}$$
$$P_{sw} = \cancel{2} \cdot f_{sw} \frac{\mathbf{E_{sw}}}{\cancel{2}}$$



Case 2: $f_{sw}(3L) = f_{sw}(2L)/2$

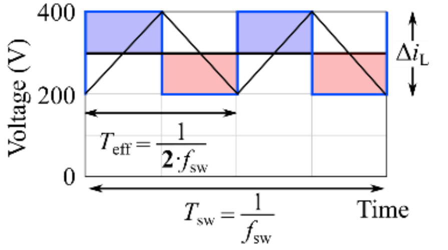
- lower losses of semiconductors
- smaller L and EMI filter

$$P_{cond} = I_{rms}^2 \mathbf{R_{on}}$$
$$P_{sw} = f_{sw} \mathbf{E_{sw}}$$



2x smaller + lower losses

$$P_{cond} = \cancel{2} \cdot I_{rms}^2 \frac{\mathbf{R_{on}}}{\cancel{2}}$$
$$P_{sw} = \cancel{2} \cdot \frac{f_{sw}}{2} \frac{\mathbf{E_{sw}}}{\cancel{2}}$$

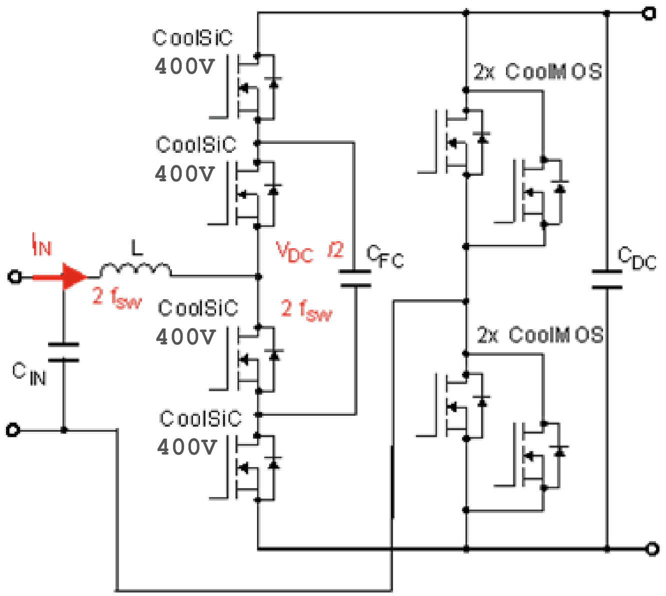


Courtesy ETH Zurich

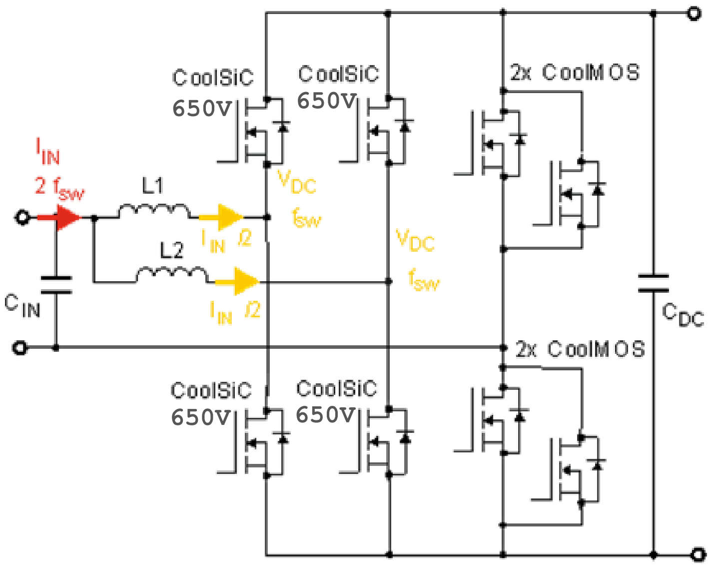
Design aspects and efficiency

- to increase power density, three main design aspects must be considered: EMI, PFC choke, bulk capacitor
- the interleaved totem-pole PFC offers a doubling effect in the frequency, enabling EMI filter volume reduction
- in addition, the 3LFC PFC requires only one PFC choke with 60% of the volume of the iTP chokes
- the 3LFC PFC efficiency is higher thanks to the lower switching losses, despite using lower-ohmic devices

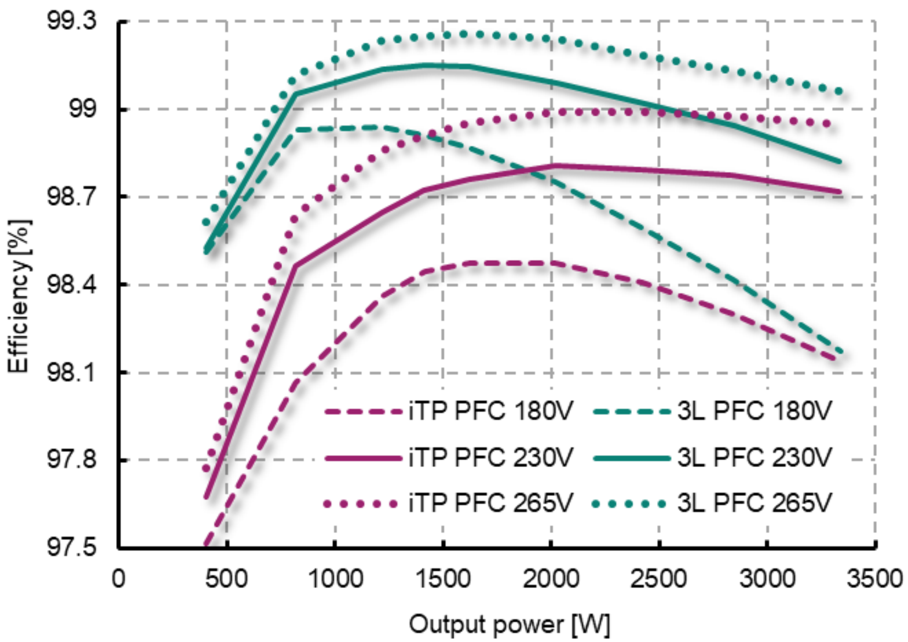
3-Level Flying Capacitor PFC



Interleaved Totem-Pole PFC

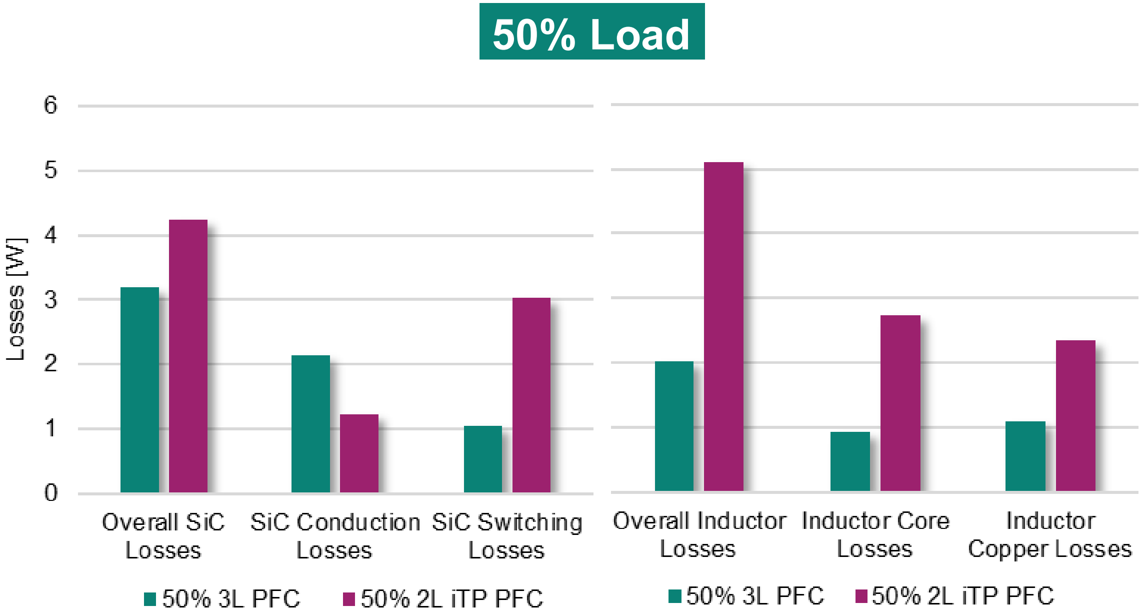


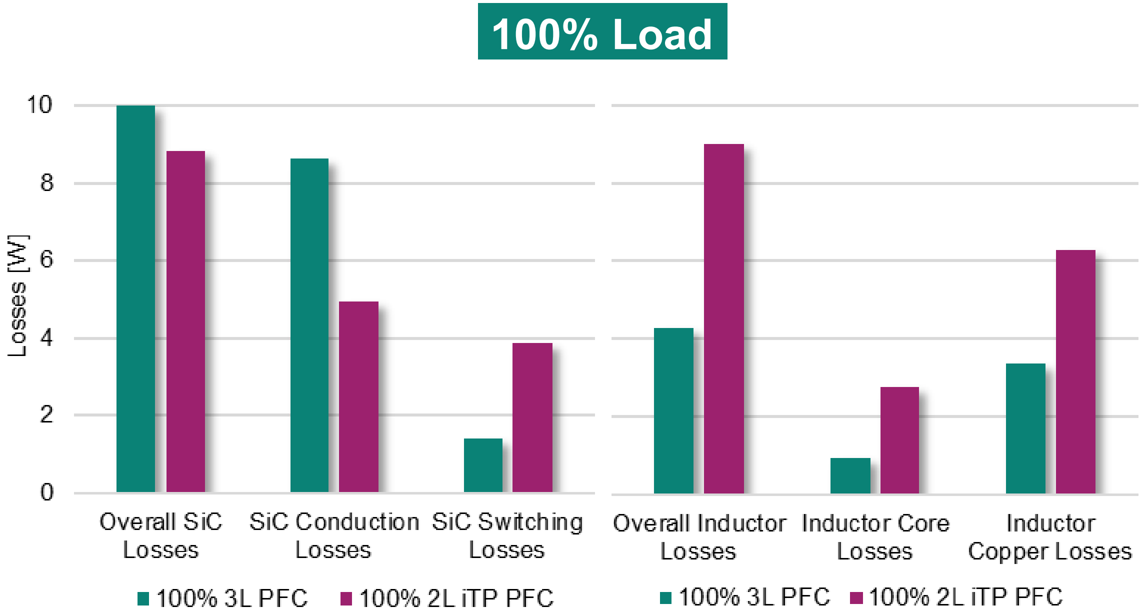
Measured Efficiency Comparison



Estimation of the loss distribution

- 3LFC PFC inductor losses are lower due to the volt-second reduction and the use of thicker wires
- 3LFC PFC shows lower SiC losses at 50% load, thanks to the lower switching losses of the 400 V devices
- at full load, the conduction losses in the 400 V devices increase, and the total losses become comparable
- losses due to EMI, relay, bulk capacitor and the SJ devices are not listed, as they are identical for both designs

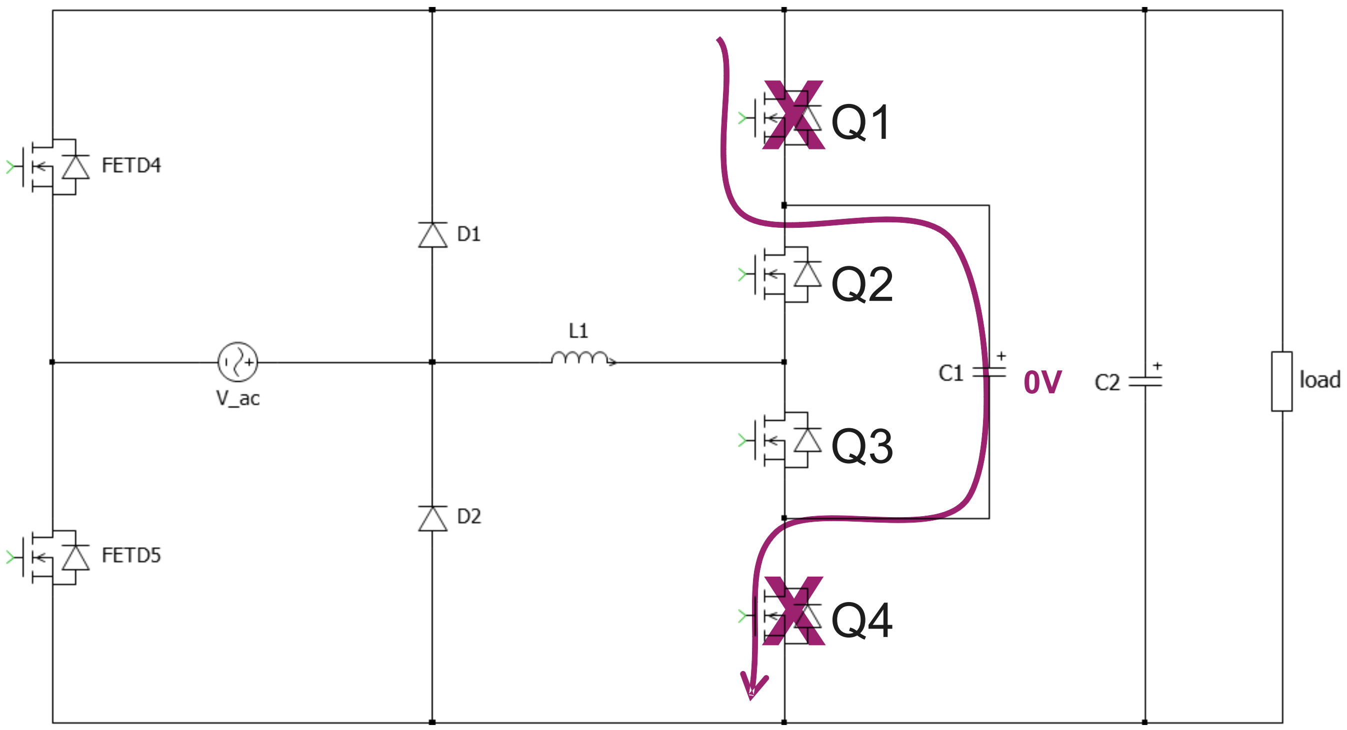




Challenges of 3-Level Flying Capacitor Designs

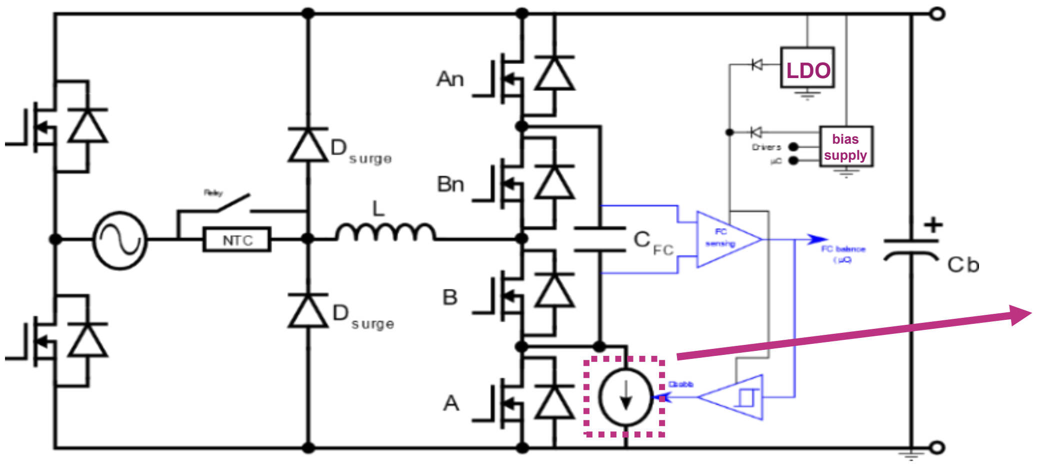
Startup Challenge – How to charge the Flying Capacitor

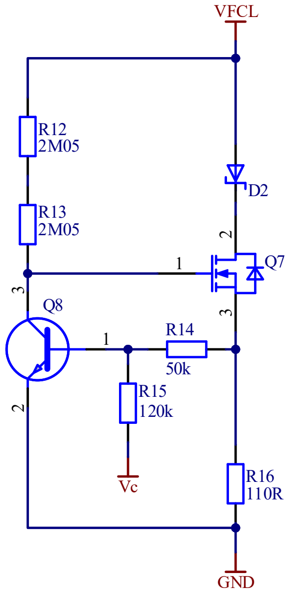
- **flying capacitor not charged at start-up**
  - bulk voltage (V_{DC}) is charged through the AC rectifier formed by D1-D2 and the body diodes of FETD4 - FETD5
  - current path for Flying Capacitor (FC) is blocked by outside devices body diodes when applying AC voltage → V_{FC} = 0 V !
- **result**
  - outside devices have to block the peak of the AC-grid voltage → **for $V_{ac,rms}$ = 305 V means $V_{DC,pk}$ = 431 V**
  - V_{DS} > 400V is applied on outer MOSFETs (not inner)

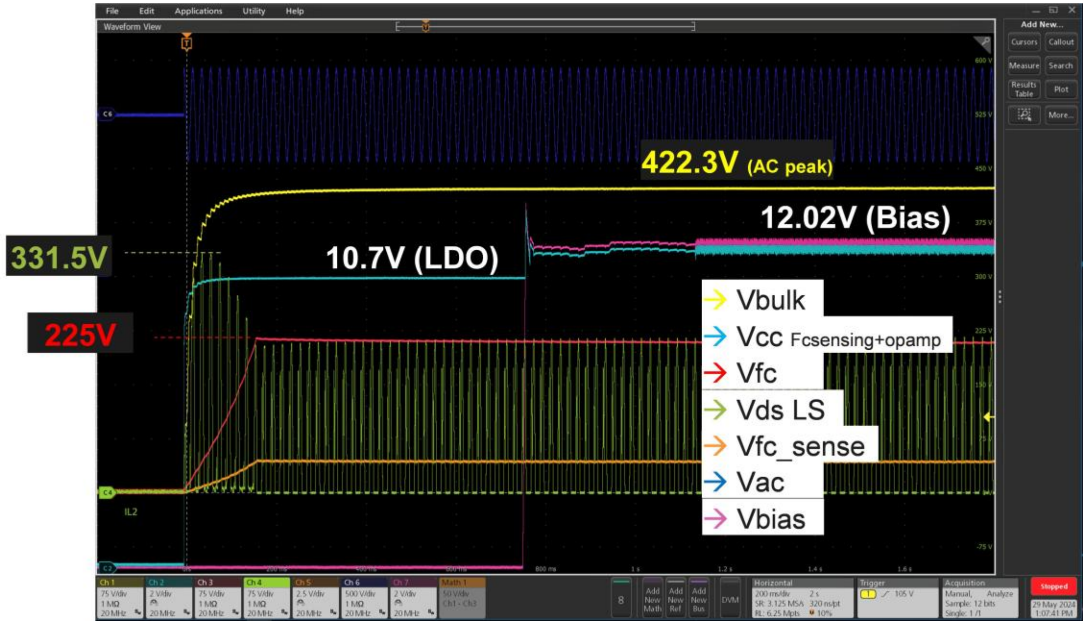


Active Precharging of the Flying Capacitor at Startup

- AC-DC and DC-AC operation (for both grid-connected and stand-alone)
- current path enabled with rising of bulk voltage, NTC in AC path to slow-down bulk voltage rise
- comparator disables current path during steady-state operation
  - no control dependency
- linear regulator to supply FC sensing, comparator and optocoupler (no bias dependency)
- no control intervention during start-up, and no firmware intervention needed



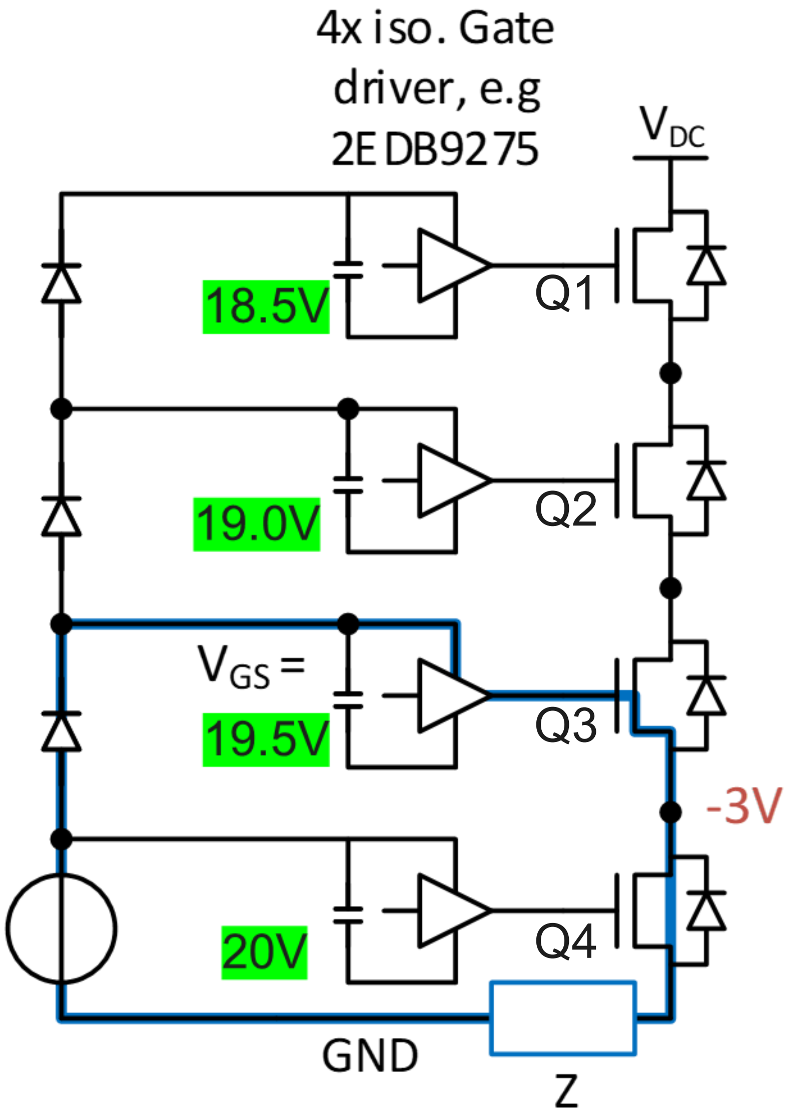




Bootstrapping in Multi-Level Flying Capacitor Systems

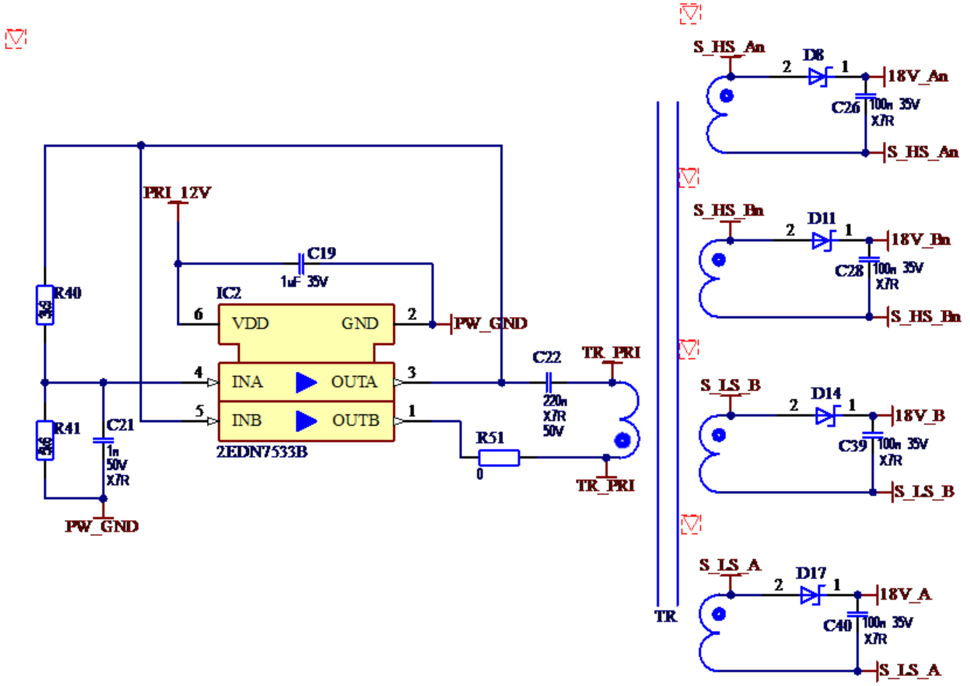
- high-side devices are supplied by **bootstrapping scheme**
- additional capacitance introduced by bootstrap diode is low
- straightforward implementation with **low cost and complexity**
- two *complementary* concerns usually arise:

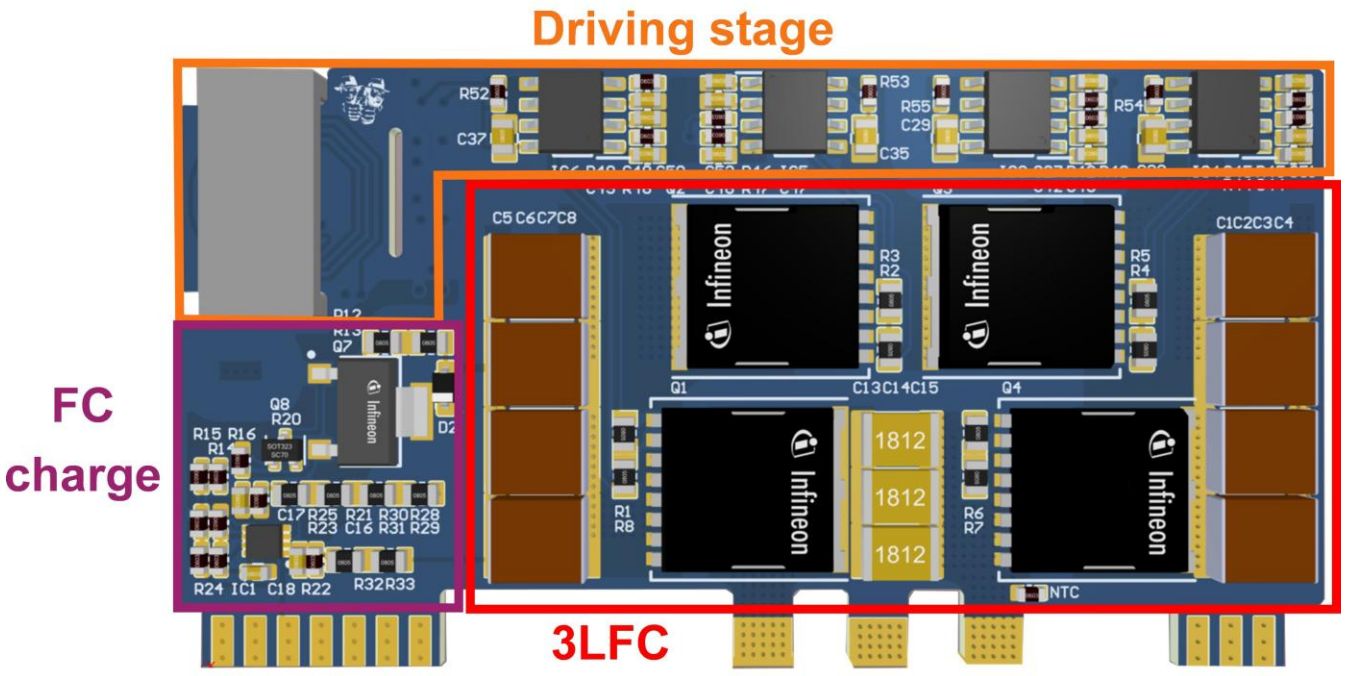
1. Over-charging
   - caused by higher forward voltage of SiC MOSFET compared to bootstrapping diode
   - commonly not a concern for a well-tuned converter where deadtimes are short
   - loop impedance limits current
2. Under-voltage
   - gate-source supply decreases by each level with Vf (~0.5V)
   - problem exacerbates with higher number of levels
   - no significant problem for SiC, due to low number of levels and some margin in V_{GS}
   - $V_{GS,max}$ with wide margin, making bootstrapping attractive ($V_{GS,max}$ = 23V)



Isolated driver supply

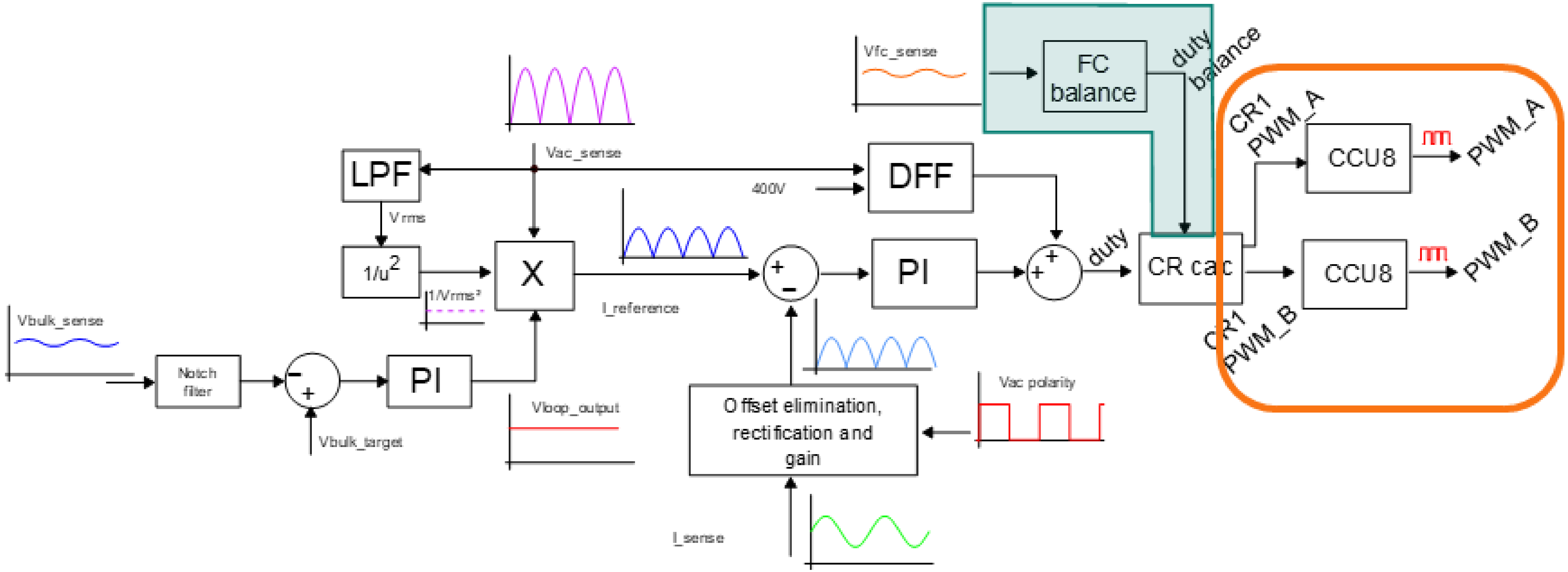
- oscillator with multiwinding transformer embedded in PCB
  - board area as design option (fit into power board)
  - inexpensive ferrite core (EQ14.5)
  - simple unipolar gate driving
- good balance of cost vs. system complexity
  - all drivers supplied -> easy and proven handling of abnormal and dynamic conditions





Control implementation

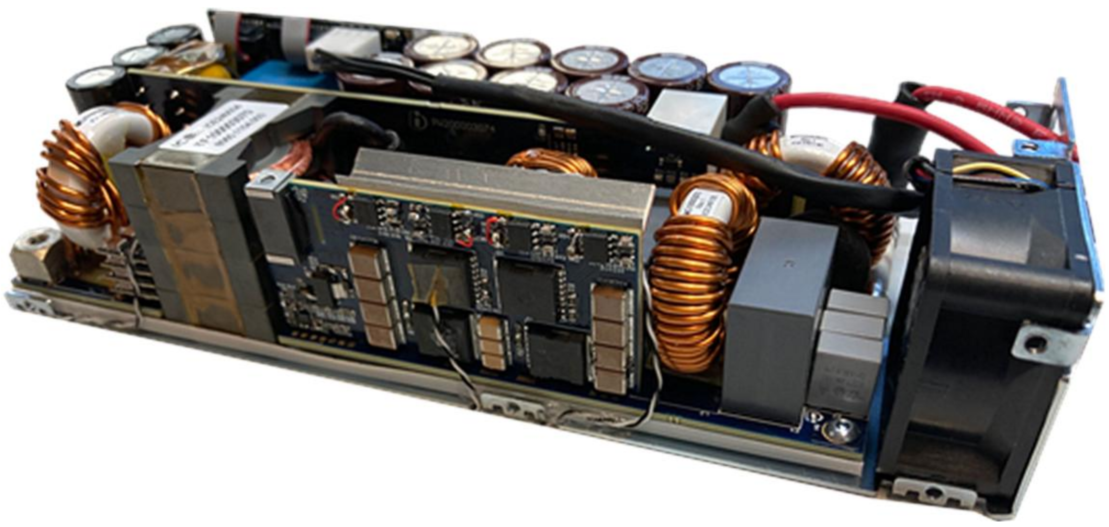
- 3-Level FC PFC uses the same PFC control architecture as the 2-Level interleaved TP PFC
- additional **V_{FC} balancing P-controller** with control variable D (ΔD << 1%) complements the natural/inherent AC cycle V_{FC} balancing



High Power Density Power Supply with 3-Level Flying Capacitor PFC

Overview of the 3.3 kW Server Power Supply with 3LFC PSU

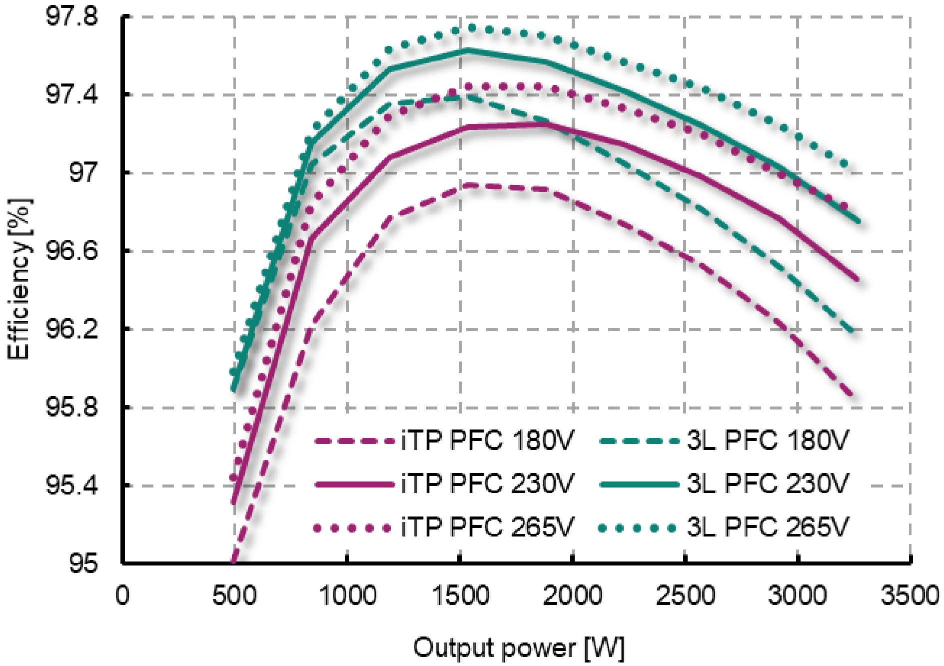
- high-efficiency PSU with 97.52 % peak efficiency (incl. fans) @ > 100 W/in^3 in 1U form factor
- complete unit with startup, FC-precharging and voltage balancing, and an isolated gate drive
- full digital control of PFC and DCDC stage supporting dynamic tests
- hold-up time extension using baby-boost (line-cycle drop-out)



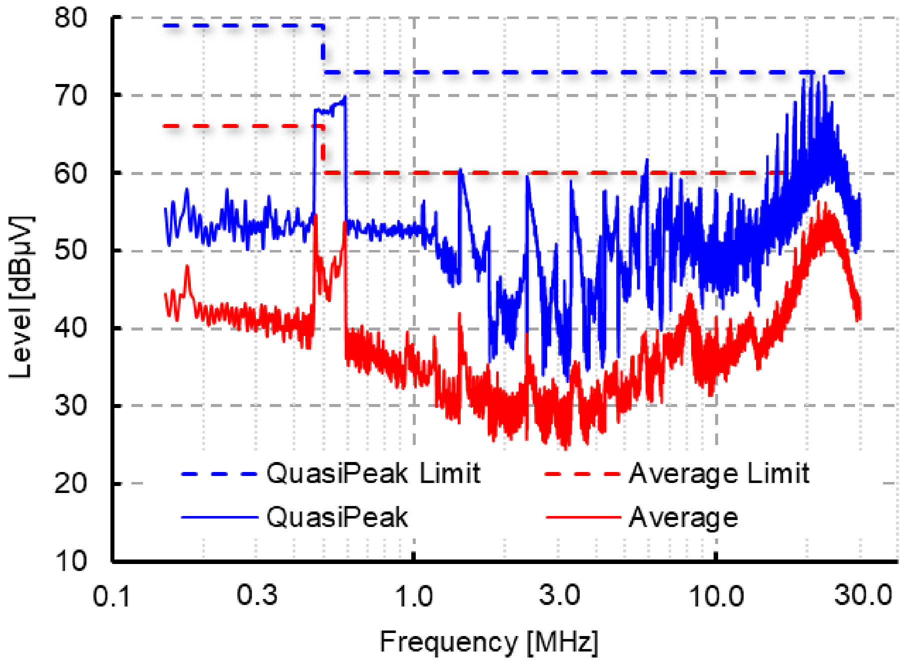
Overall efficiency and EMI

– peak efficiency of the PSU with 3LFC PFC achieved at half-load and nominal input voltage of 230 V
– compared to the 2L TP PFC, the efficiency improves by > 0.2 % over the entire load range, with a peak improvement of 0.5 % at light load condition
– EMI measurements, in a non-certified test bench with LISN and resistive load, proof compliance with CISPR 22/32 / EN55022 standards

Overall Efficiency of the Power Supply



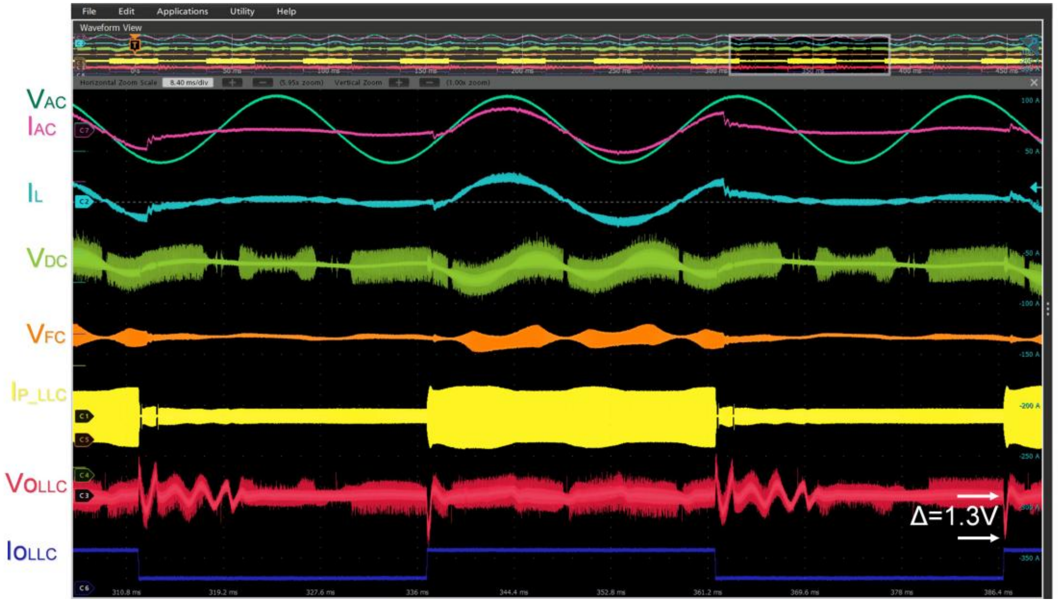
Average and Peak EMI Measurement



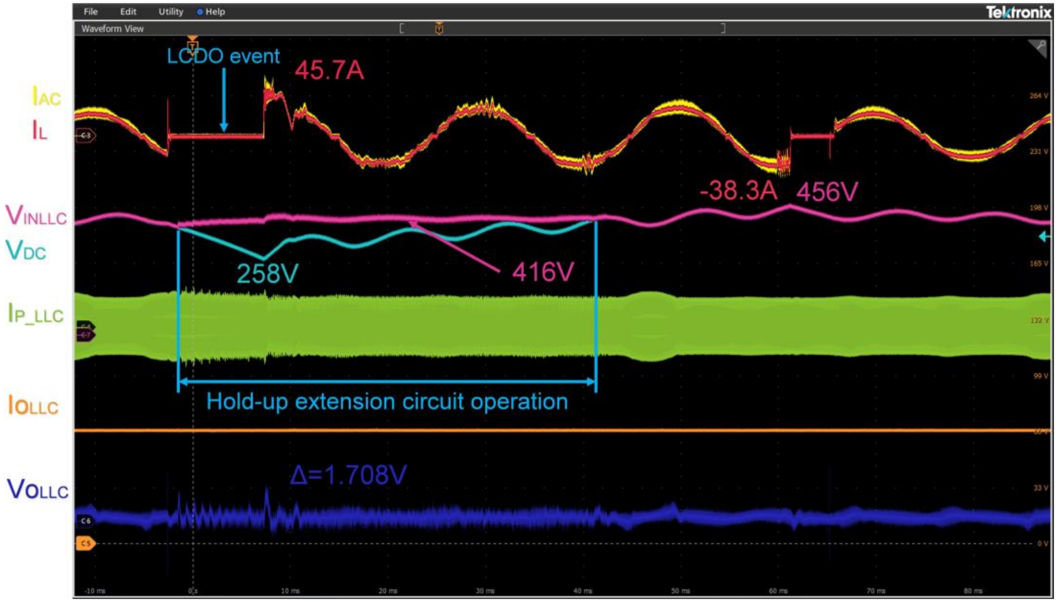
Ruggedness to Power Line Disturbances

- the power supply yields a stable behavior in case of dynamic load change from 500 W to 3300 W with 1 A/µs for every 25 ms
- FC voltage remains balanced, and LLC output varies with less than 3 % of the nominal output voltage
- the unit is capable to support a 10 ms hold-up time at full load in case of line-cycle drop out

Dynamic Load Change: 500 W -> 3300 W



Line-cycle Drop Out: 10 ms at Full Load



Summary

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- the 3-Level Flying Capacitor CCM Totem-Pole PFC with CoolSiC 400 V MOSFET is a very attractive solution for high efficiency and high power density
  - switching Figure-of-Merits and on-state resistance offer clear benefits over 650 V devices
  - 3L topology enables higher blocking voltage especially in data centers at 277 V and above
  - inherent frequency multiplication and lower voltage swings enable smaller inductors and EMI filter
  - distributed losses and the very flat R_{DSon} over temperature enables the use of higher R_{DSon} devices for further cost reduction

- an outstanding PFC efficiency of 99.2 % at 230 V is demonstrated

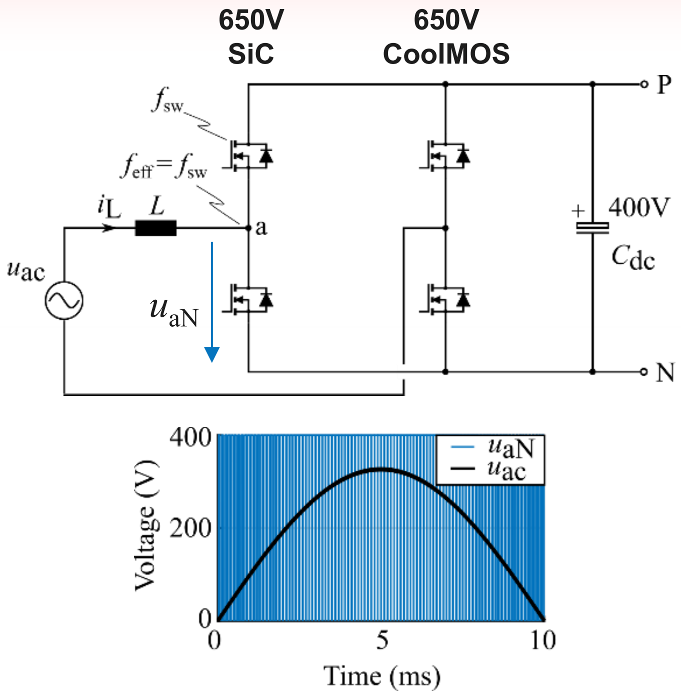
- the proposed solution successfully addresses several challenges like balancing of the flying capacitor voltage or managing the start-up and shows excellent ruggedness towards power line disturbances

- complete power supply shows an excellent peak efficiency of 97.52 % (incl. fans), and provides a high power density beyond 100 W/in^3 in a common 1U form factor

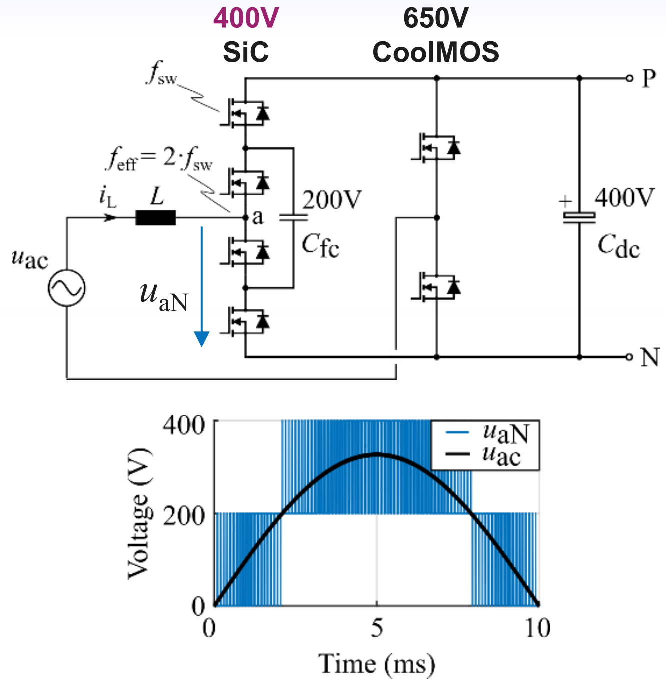
Infineon

2-Level vs 3-Level Totem-Pole PFCs

2-Level



3-Level

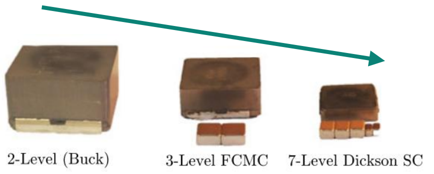


(N = #Levels -1)

Multi-Level

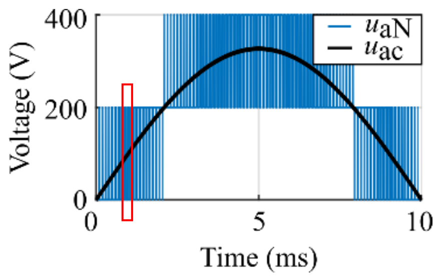
1) **Switching Freq. Multiplication** → $f_{sw,eff} = N \cdot f_{sw}$
2) **Staircased Voltage Waveform** → **"Multi-Level"**
3) Use of **LV Semiconductors** → **Better FOM**

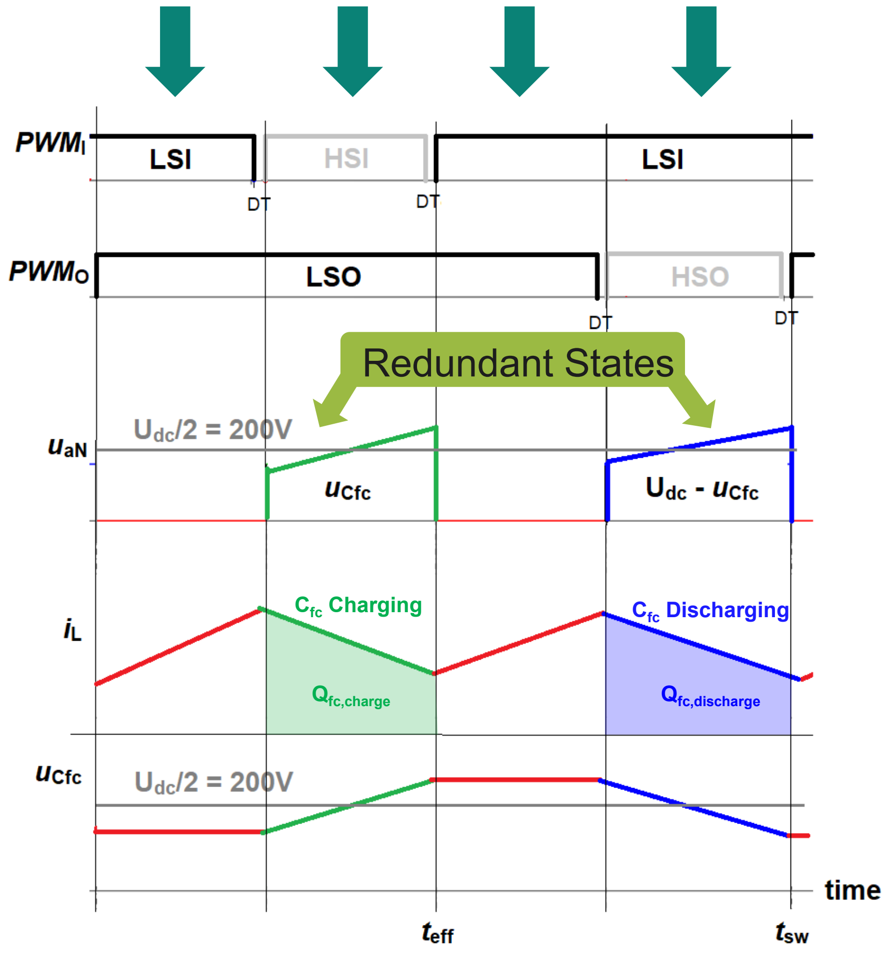
Reduce Magnetics & Filter Volume

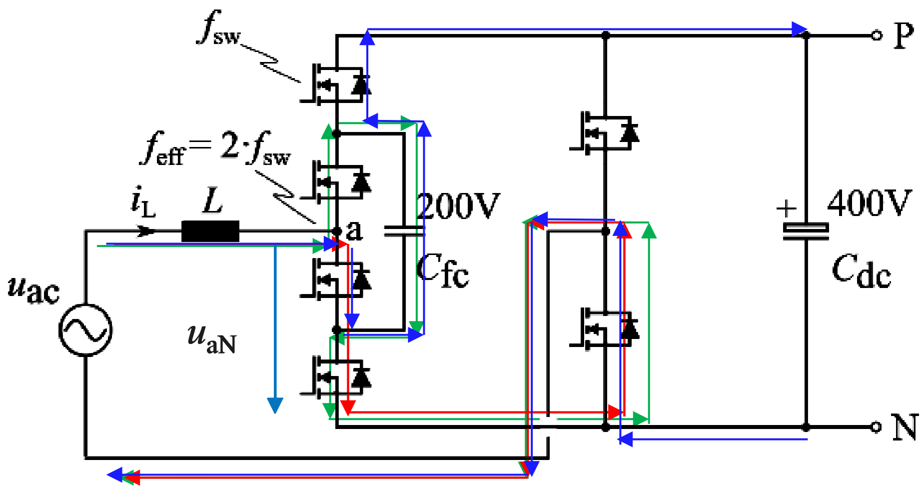


[Y. Lei, R.C. N. Pilawa et al.,"An Analytical Method to Evaluate and Design Hybrid Switched-Capacitor and Multilevel Converters", IEEE TPEL, 2018]

3-Level Half-bridges and Series-interleaving:
Operation for D < 0.5





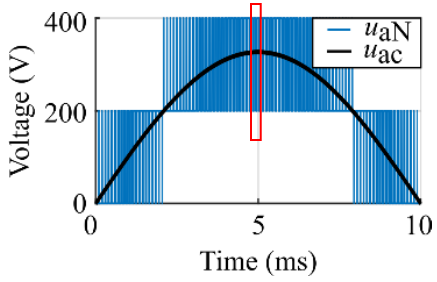


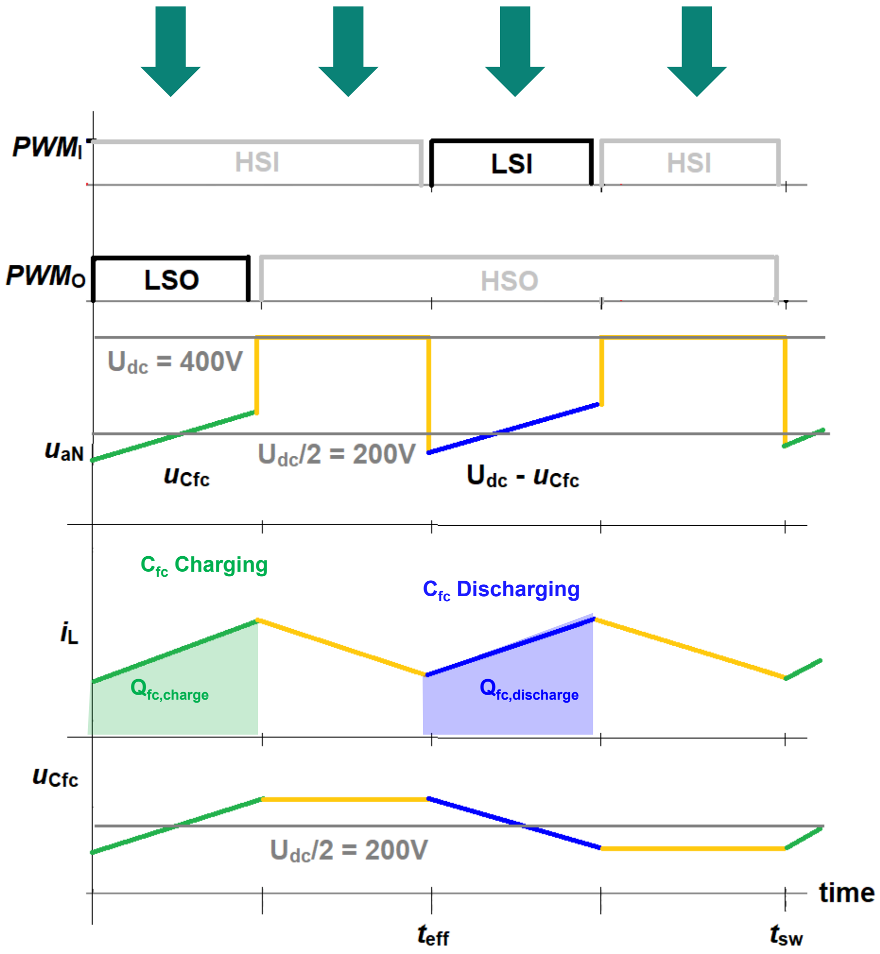
Tip:

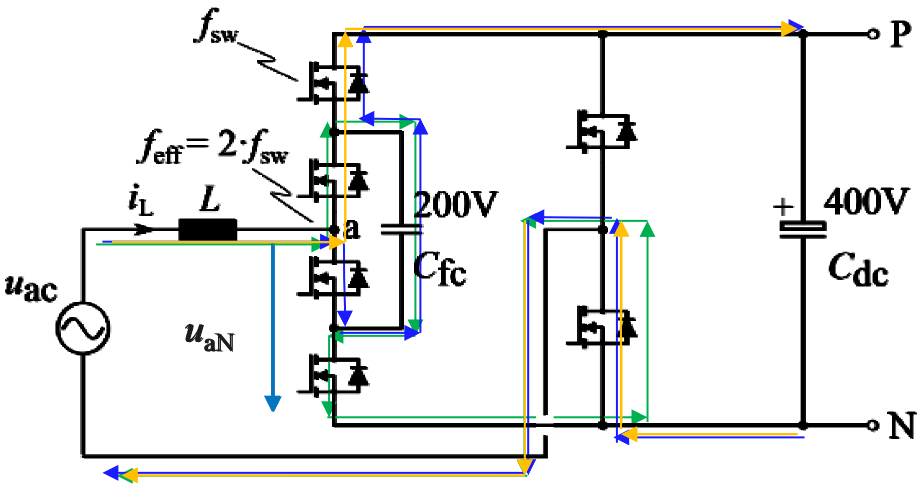
- Duty-cycles of HSI and HSO affect the ripple current Δi_L and the charge through C_{fc} - $Q_{fc,charging}$ and $Q_{fc,discharging}$
- By controlling $Q_{fc,charging}$ and $Q_{fc,discharging}$, the u_{Cfc} can be controlled!

Balancing of flying capacitors by adjusting the lengths of the redundant states!

3-Level Half-bridges and Series-interleaving:
Operation for D > 0.5







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