Research on Overcurrent Interruption Capability and Influencing Factors of SiC MOSFETs in DCCBs

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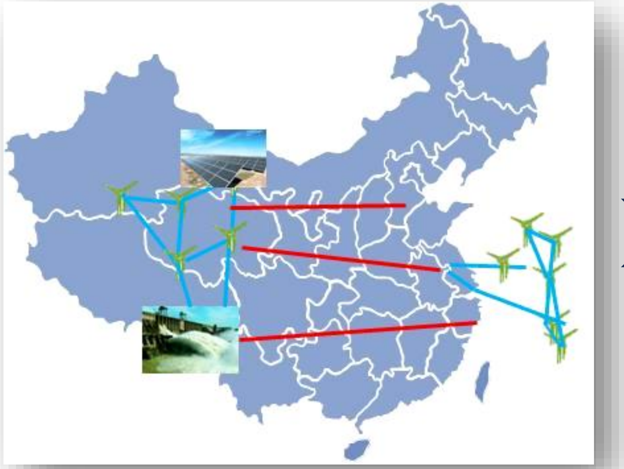
Content

➢ Introduction

- ☐ Flexible DC grids' low impedance causes rapidly rising fault currents, necessitating DCCBs for millisecond-level fault interruption.
- ☐ Power modules are the core component of high-voltage DCCB.

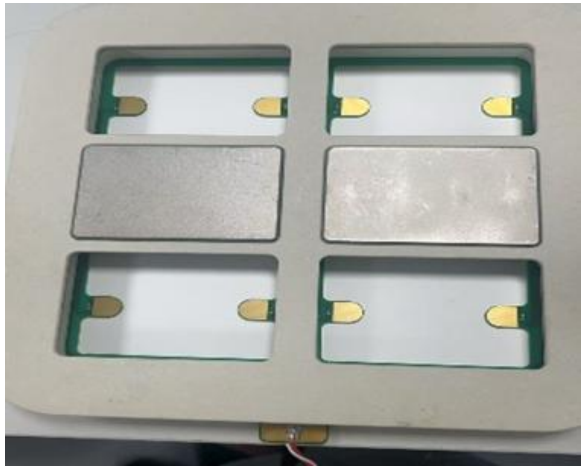


Flexible direct current transmission

- Flexible Dispatch
- Efficient Transmission
- Facilitated Renewable Energy Grid Integration

DC circuit breakers

- Short switching time
- High on-state current
- High withstand voltage



Power modules

- High voltage and high current
- Fully-controlled and high reliability
- High-temperature capability and low losses

➢ Introduction

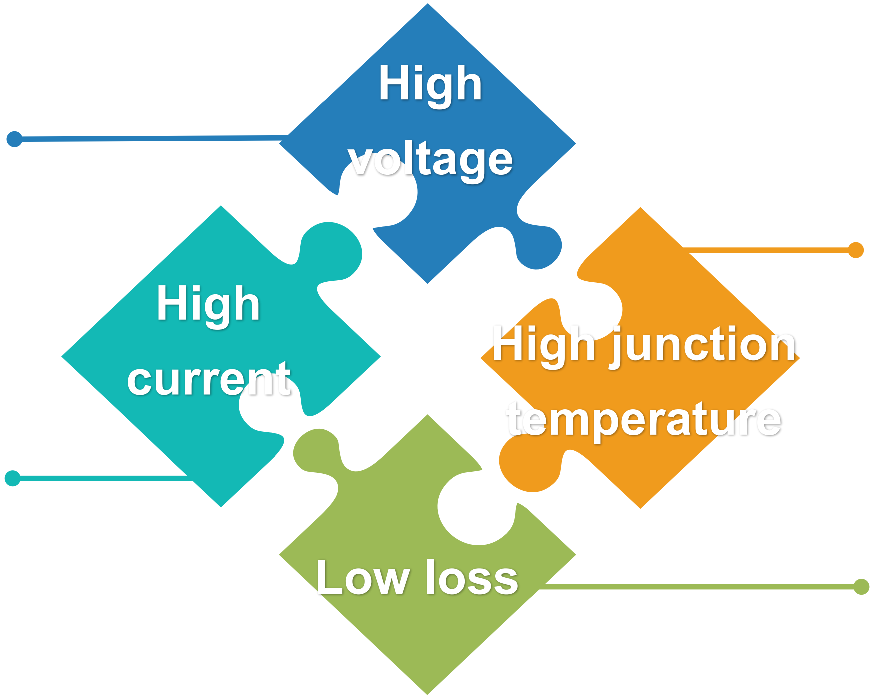
☐ Silicon-based devices suffer from low efficiency and bulkiness, failing practical new electricity system. This necessitates next-generation power devices with **higher voltage/current capabilities, elevated junction temperatures, and lower losses** for essential system support.

■ **Higher voltage**

Reduce the number of devices in series and optimizes the topology.

■ **Higher current**

Improve the fault traversal ability and reliability of the system.



■ **Higher junction temperature**

Simplify the equipment's heat dissipation system and reduce overall system costs.

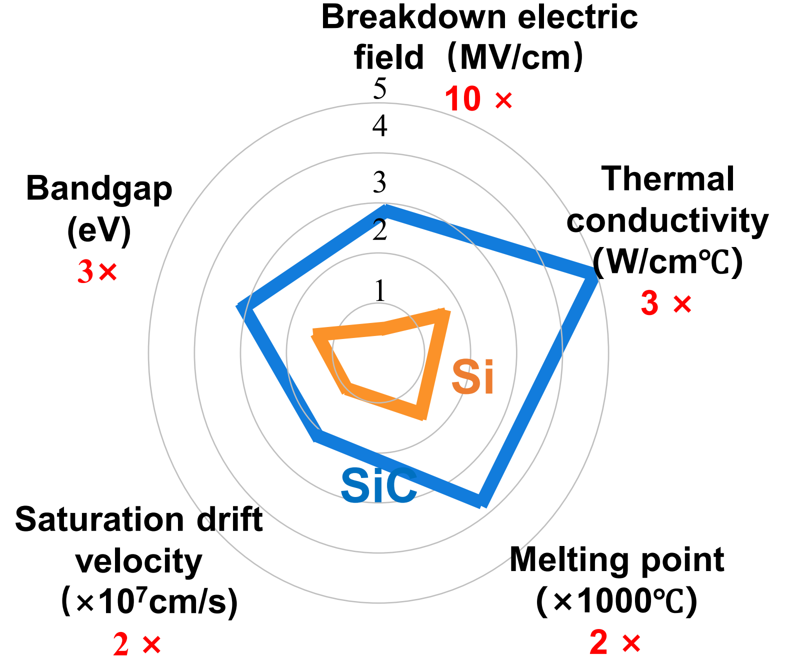
■ **Lower loss**

Reduce system heating; Improve the efficiency of system transmission and conversion.

Advanced Requirements for Power Devices in High-Efficiency Power Electronic Transformers

➢ Introduction

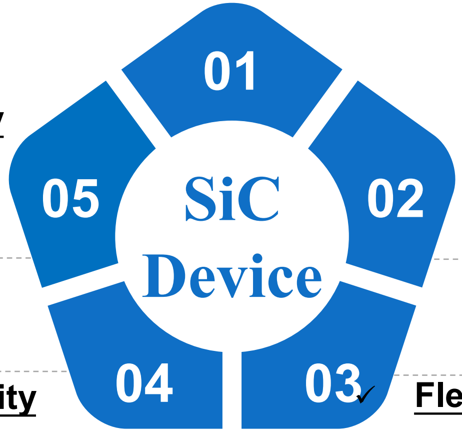
- SiC's superior material properties enable high-voltage, high-temp, low-loss power devices vs. Si.
- SiC devices increase DCCB efficiency and power density, reduce volume, and strengthen technical advantages for future DC grids.



SiC vs. Silicon: Property Comparison

- ✓ **Simplified system design**
- ✓ The number of devices connected in series is reduced by 60%

- ✓ **Enhanced efficiency**
- ✓ Reduce energy loss by more than 60%



- ✓ **Reduced footprint**
- ✓ Device volume halved; footprint reduced by 50%

- ✓ **Improved reliability**
- ✓ Simplify the system design and enhance reliability

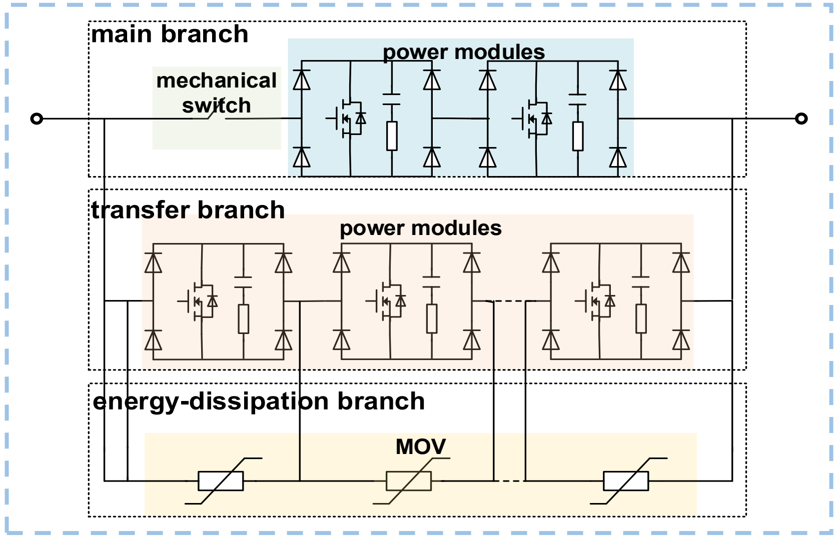
- ✓ **Flexible power delivery control**
- ✓ Increase the flexibility and controllability of power transmission

SiC-Enabled DCCBs

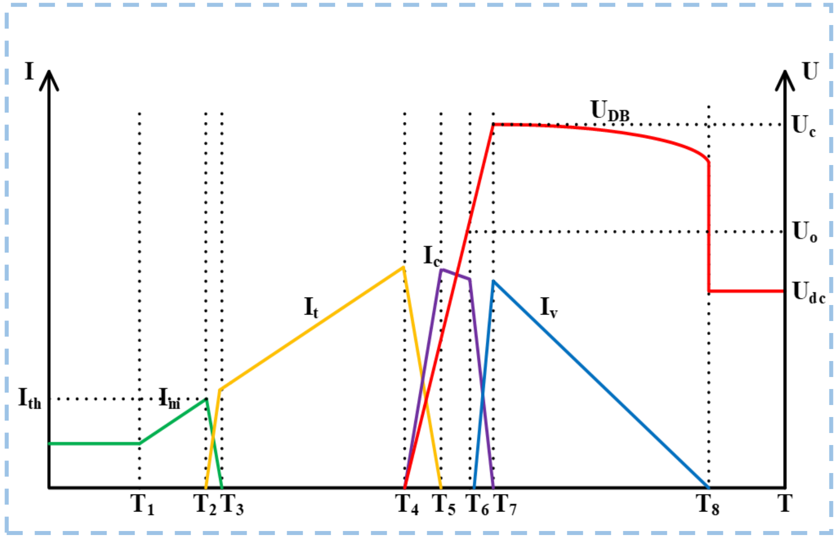
➢ Overcurrent Interruption Capability Comparison

◆ Topology and Principles of Hybrid DCCBs

- Main Branch: Fast mechanical switch + few power modules (**conducts load current**).
- Transfer Branch: Multi-level series power modules (**carries/interrupts fault current**).
- Energy-Dissipation Branch: Series MOVs (**limits overvoltage, absorbs inductive energy**).



Topology of the hybrid DCCB



Principle of the hybrid DCCB

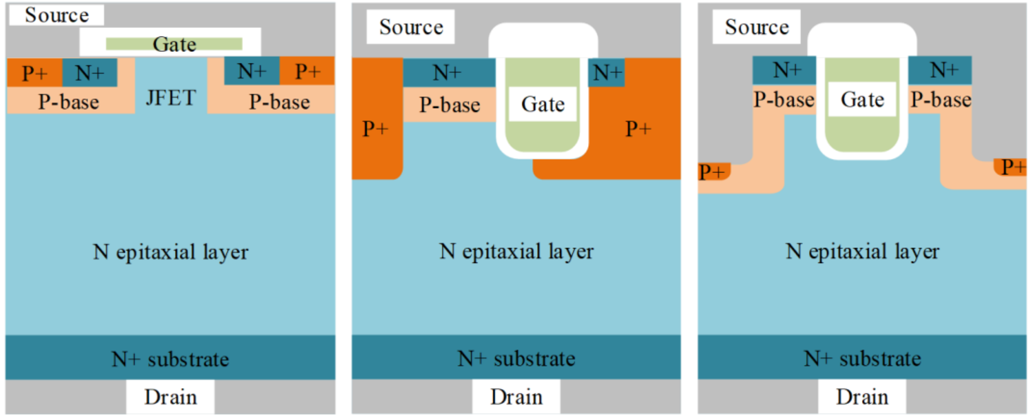
➢ Overcurrent Interruption Capability Comparison

◆ Experimental Setup

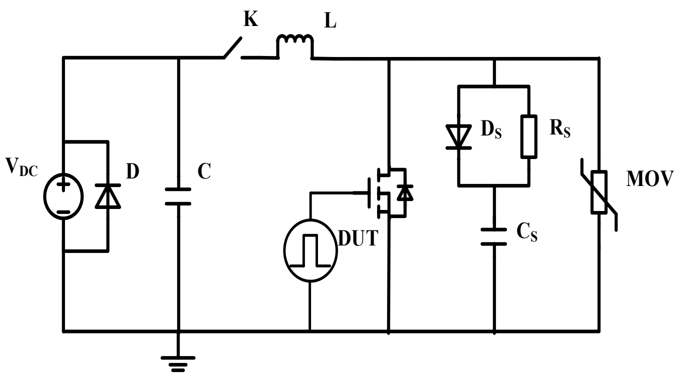
- ✓ Planar (1200 V/ 57 A/ 39 mΩ)
- ✓ Asymmetric trench(1200 V/ 55 A/ 40 mΩ)
- ✓ Double trench (1200 V/ 55 A/ 40 mΩ)

Power devices in DCCB Transfer Branch :

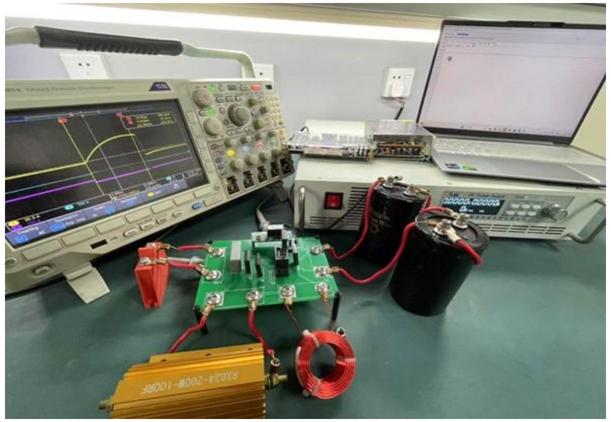
- ✓ Withstand above-rated short-circuit currents (ms)
- ✓ Conduct → interrupt sequence
- ✓ most demanding tests



Cell structures of three DUTs



Experiment circuit



Experiment platform

➢ Overcurrent Interruption Capability Comparison

◆ Comparison results of overcurrent interruption capability

U_{ds}↑ with I_{ds} ↑& T_j ↑ ⟺ T_j ↑ with I_{ds} ↑ & U_{ds}↑

Distinct knee point = Linear → Saturation transition

Key Limiters of OC:

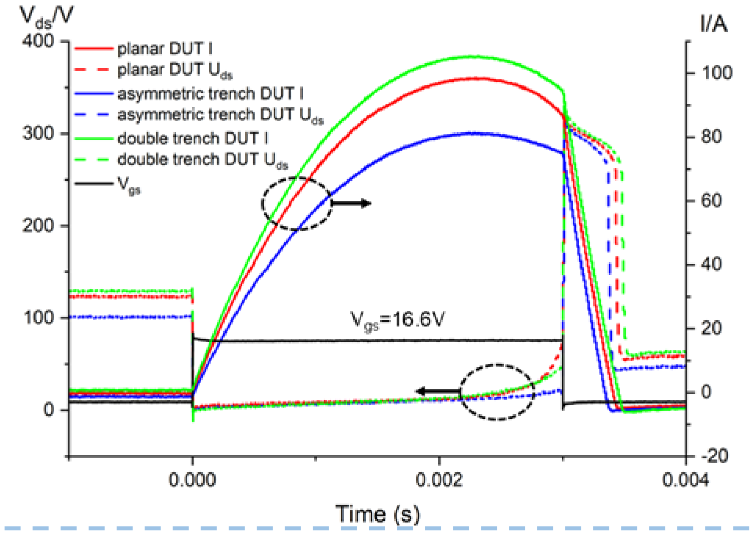
R_{on} 、 I_{sat}

$$P_{max} = \frac{T_{jmax} - T_c}{R_{th}} \quad (1)$$

$$R_{th} = \frac{d}{\lambda A} \quad (2)$$

Chip area↑ ⟹ overcurrent ↑

Trench structure ⟹ overcurrent density ↑



DUTs	I_{rated} (A)	I_{max} (A)	I_{norm}	I_{avg} (A/mm²)
Planar	57	99.2	1.74	11.69
Asymmetrical	55	83.4	1.51	15.58
Double	55	106.1	1.92	17.32

The comparison of the maximum overcurrent of the three DUTs

➢ Overcurrent Interruption Capability Comparison

◆ Comparison results of overcurrent interruption capability

SiC MOSFET OC Comparison (DCCB):Planar vs. Asymm. Trench vs. Double. Trench

✓ Overcurrent density Ranking

- 🥇 Double Trench: Highest OC density
- 🥈 Asymmetric Trench
- 🥉 Planar

→ Trench advantage: Channel density ↑, $R_{ON,sp}$ ↓

✓ Turn-off Capability Ranking

- 🥇 Double Trench: Superior performance
- 🥈 Planar
- 🥉 Asymmetric Trench: Thermal bottleneck

→ (Small active area → heat concentration)

✓ Fundamental Limiters

⚡ R_{ON} & I_{sat} → (Primary constraints for SiC MOSFET OC capability)

➢ Factors Influencing Overcurrent Interruption Capability

- Enhancing I_{sat} & reducing R_{on} to analyze max turn-off overcurrent
- Subsequently evaluating gate voltage, environment Temperature and on-state duration effects on OC interruption capability under DCCB conditions.

R_{on}

$$R_{ON} \sim R_{ch} + R_{JFET} + R_{Drift} \quad (4)$$

$$R_{ch} = \frac{LW}{2\mu_n C_{ox}} \frac{1}{V_{gs} - V_{th}} \quad (5)$$

$$R_{JFET} = \frac{\rho_{JFET} \chi_{jP} W}{\alpha} \quad (6)$$

$$R_{Drift} = \frac{L_d}{q\mu_{n\_d} N_d A_d} \quad (7)$$

I_{sat}

$$I_{sat} = \frac{W\mu_n C_{ox}}{2L}(V_{gs} - V_{th})^2 \quad (3)$$

Influence Factors:

Gate Drive Voltage

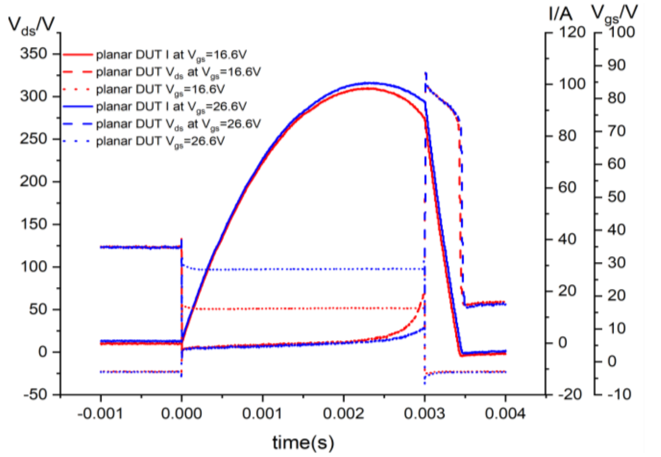
Environment Temperature

On-State Duration

➢ Factors Influencing Overcurrent Interruption Capability

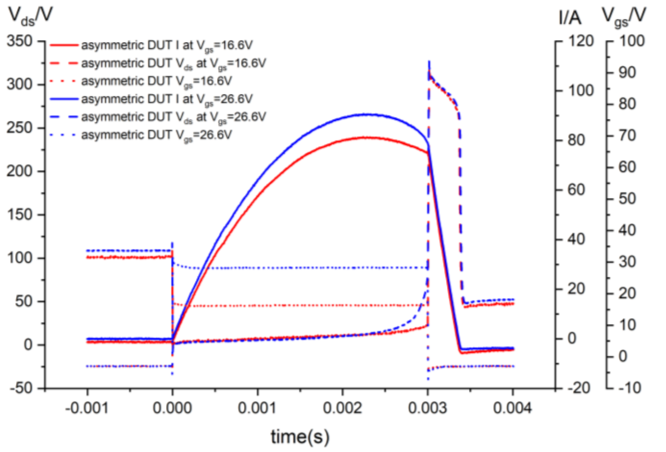
◆ Influence of Gate Drive Voltage

- ☐ Planar DUT: Thermal failure → Gate-source short (thin gate oxide)
- ☐ Trench DUT: Higher sensitivity to V_{gs} (trench structure & process)
- ✓ Dry etching → Interface defects R_{CH}↑ I_{sat}↓
- ✓ V_{gs} ↑: Inversion charge accumulation R_{CH} ↓ contribution to R_{on}
- ✓ Higher trench density → Key to I_{sat} ↑



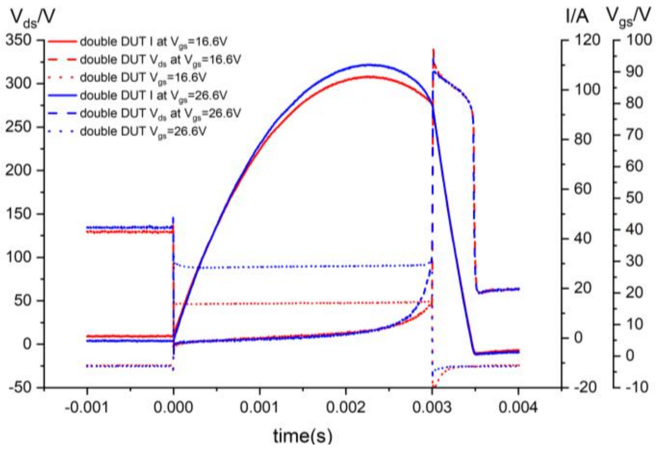
16.6V→26.6V OC 1.6%↑

Planar DUT



16.6V→26.6V OC 9.8% ↑

Asymmetric trench DUT



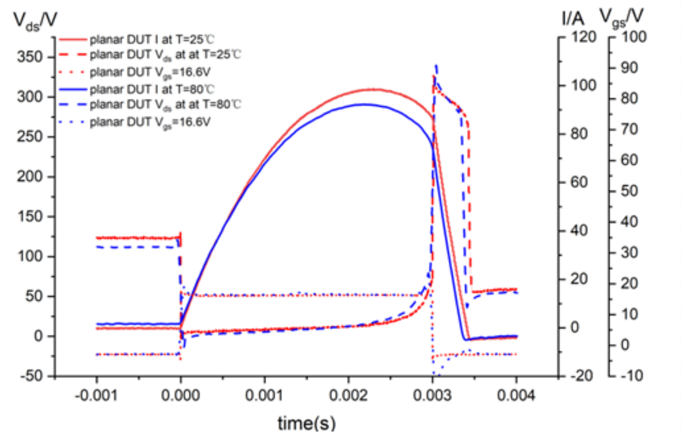
16.6V→26.6V OC 7.1% ↑

Double trench DUT

➢ Factors Influencing Overcurrent Interruption Capability

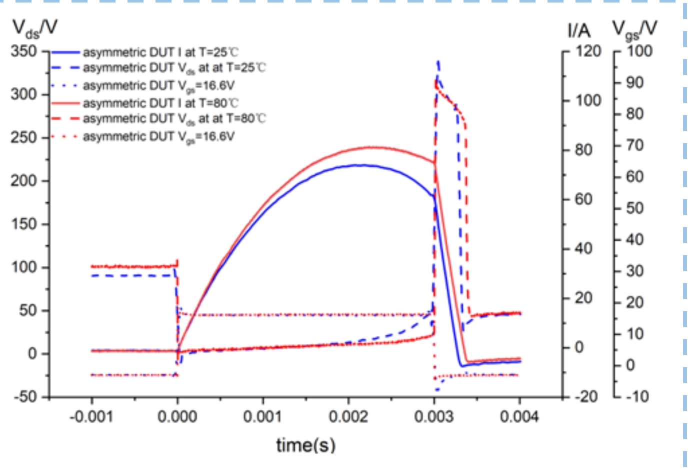
◆ Influence of Environment Temperature

- ◻ **μ_n-T Relationship: High T (>350°C): Deep traps emission↓ + Phonon scattering↑ → μ_n↓ →R_{ON}↑、I_{sat}↓**
- ◻ **Environment Temperature Influence : T_c↑ → Earlier thermal limit → OC capability ↓ (Worst in asymmetric DUT: smallest active area → heat accumulation)**



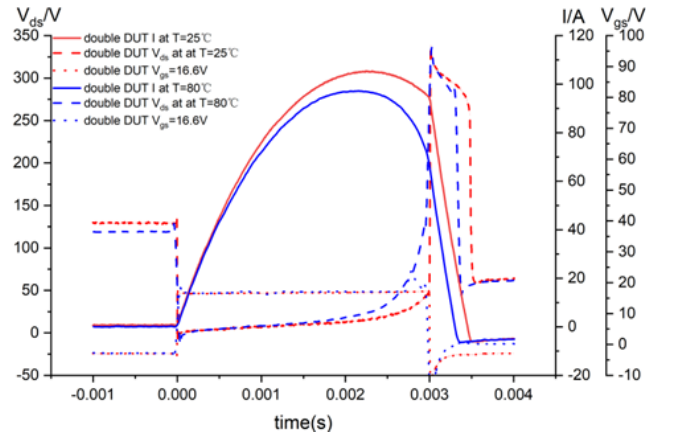
25℃→80℃ OC 7.3% ↓

Planar DUT



25℃→80℃ OC 11.7% ↓

Asymmetric trench DUT



25℃→80℃ OC 8.0% ↓

Double trench DUT

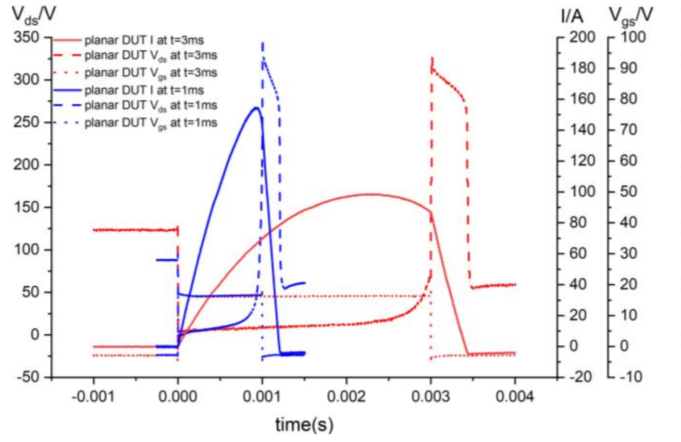
➢ Factors Influencing Overcurrent Interruption Capability

◆ Influence of On-State Duration

- ☐ On-State Duration ↑ → Energy accumulation → T_j ↑ →Latch-up effect → Failure
- ✓ (Root cause = **Temperature** → Matches external T_c trend;

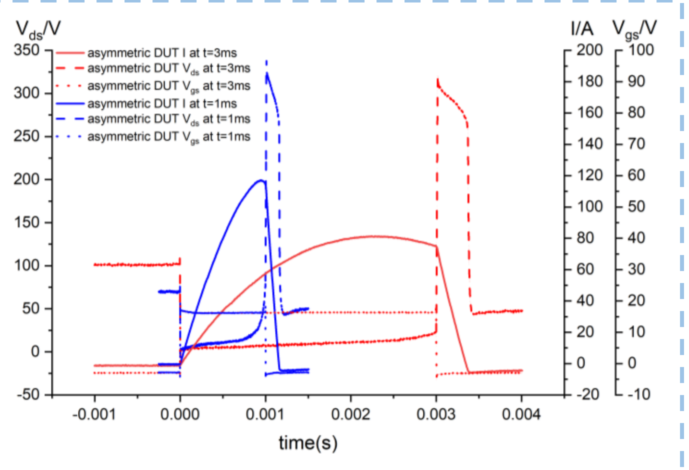
$$E = \int_0^{t_{on}} V_{ds} I_{ds} dt \tag{8}$$

- ✓ Short on-State duration impact > external T_c → Short-pulse operation: Inadequate heat dissipation→ Identifies **internal heating as decisive factor**



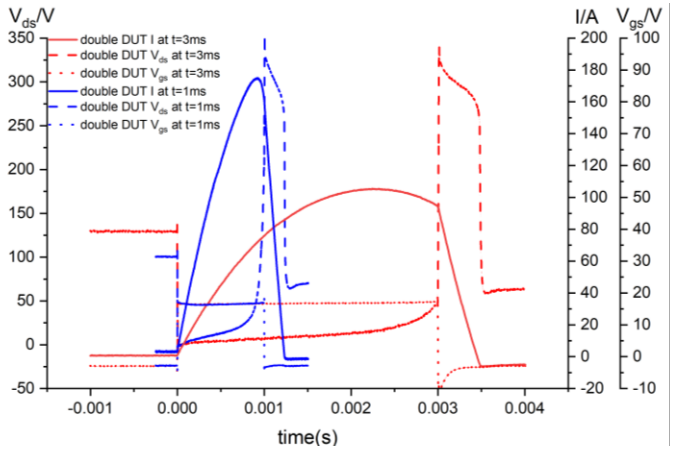
3ms→1ms OC 58.3%↑

Planar DUT



3ms→1ms OC 40.3%↑

Asymmetric trench DUT



3ms→1ms OC 64.9% ↑

Double trench DUT

➢ Factors Influencing Overcurrent Interruption Capability

SiC MOSFET OC Comparison (DCCB):Planar vs. Asymm. Trench vs. Symm. Trench | 3 Key Factor

3 Key Factor

Gate Drive Voltage

- ✓ Trench DUTs: Significant OC ↑ with V_{gs} ↑ (trench structure & process)
- ✓ Planar DUT: Gate-source short risk (Thin oxide limitation)

Environment Temperature

- ✓ All DUTs: OC↓ with T_c↑(Mechanism: with T_c ↑, Earlier thermal limit： R_{ON}↑、I_{sat}↓)
- ✓ Critical Case: Asymmetric trench (smallest active area : Thermal accumulation hotspot)

On-State Duration

- ✓ Key Finding: t_{on} ↓ → OC ↑↑ capability (Outperforms ambient T_c mitigation)
- ✓ Root Cause: Internal heat spike > ambient heating (Inadequate heat dissipation in such a short period of time)

⚠️ DCCB Design Rule: **Minimize t_{on}**

➢ Conclusion

- Current Conduction Density: Double trench > Asymmetric trench > Planar (trench designs boost channel density & reduce $R_{ON,sp}$)
- Overcurrent Interruption Capability: Double trench > Planar > Asymmetric trench(Asymmetric trench limited by smaller active area & concentrated heat dissipation)

- **Increasing gate voltage, reducing environment temperature, and shortening on-state duration enhance performance by reducing R_{ON} and boosting I_{sat} to varying degrees.**
  - ➢ Gate drive voltage boosts trench DUTs' overcurrent interruption via structural advantages, while planar DUTs face gate-source short-circuit limitations.
  - ➢ As the environment temperature increases, the overcurrent interruption capability of all DUTs declines due to the faster rise in DUTs' temperature into the high-temperature range, which increases R_{ON} and reduces I_{sat}.
  - ➢ On-state time enhances interruption capability (surpassing temperature effects) with internal loss-induced thermal rise as decisive constraint. Shortening the on-state duration is critical for improving performance.

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Thank You!

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