Analysis and Study on the Advantages of one Innovative SiC Chip Embedding PCB Solution for xEV Main Inverter Application

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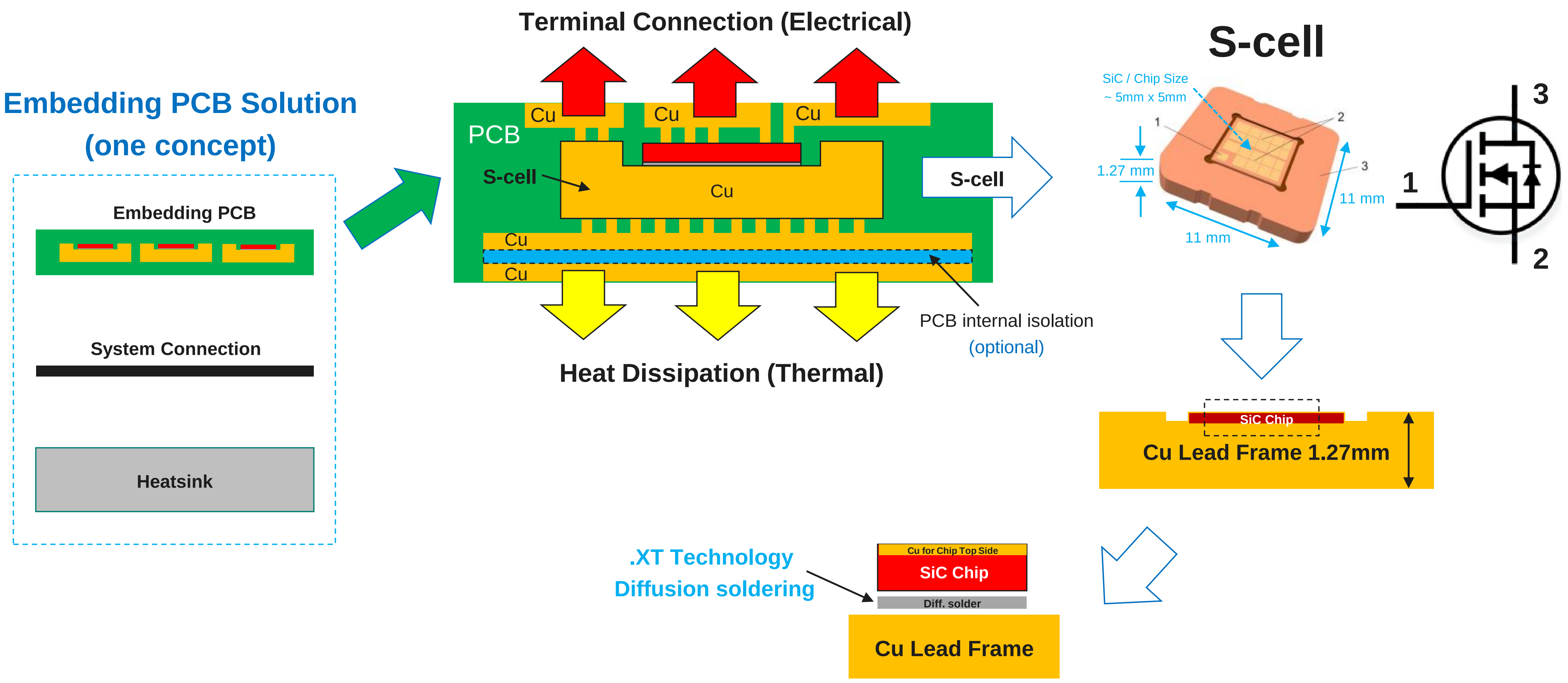
The introduction of S-cell based embedding PCB solution



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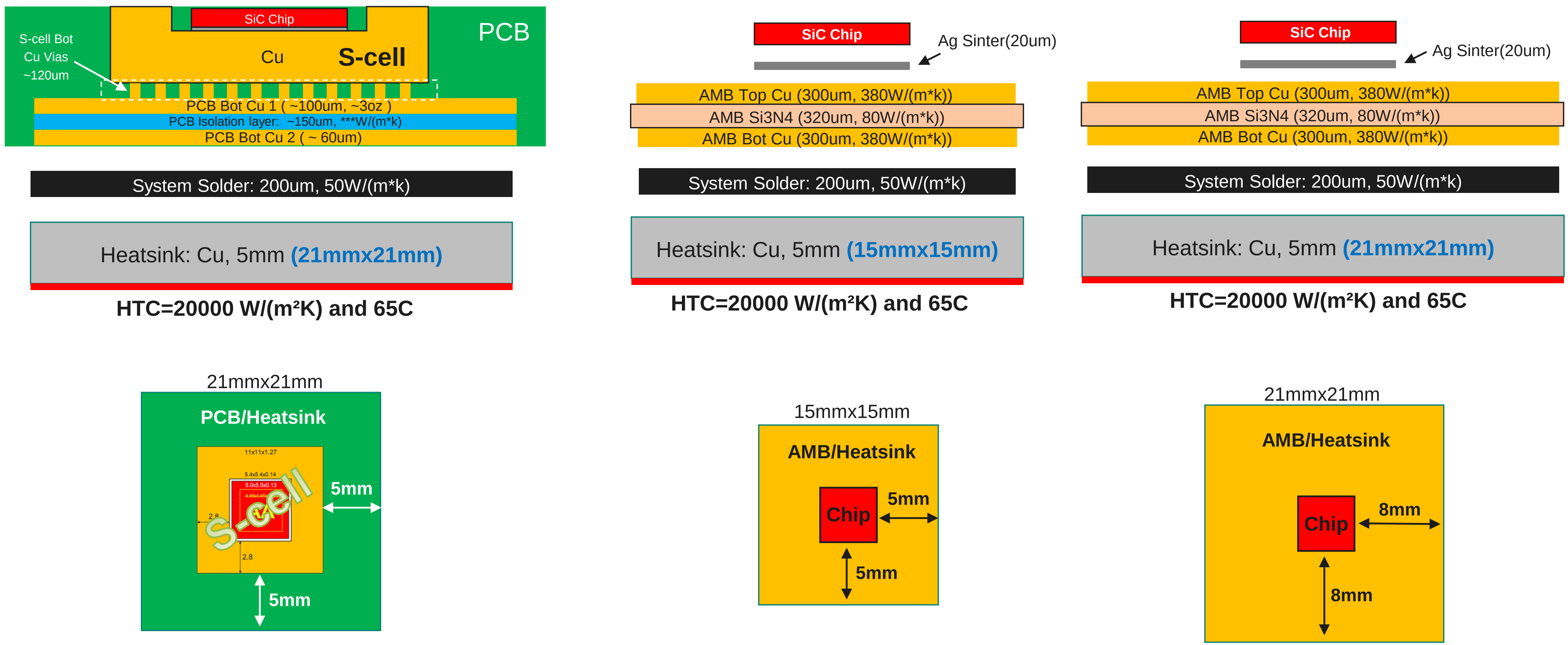
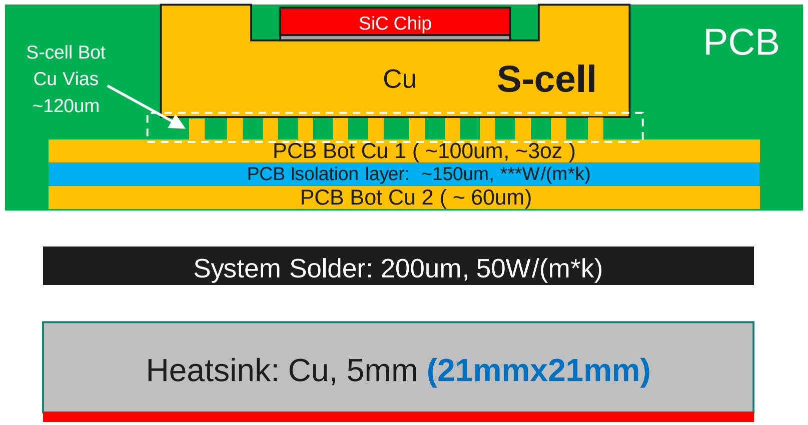
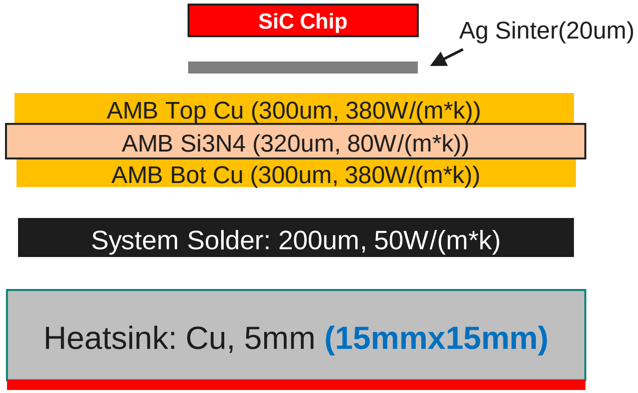
Thermal Model of Embedding PCB Solution VS Module Solution
Case 0 (not compared in the paper) → Setup



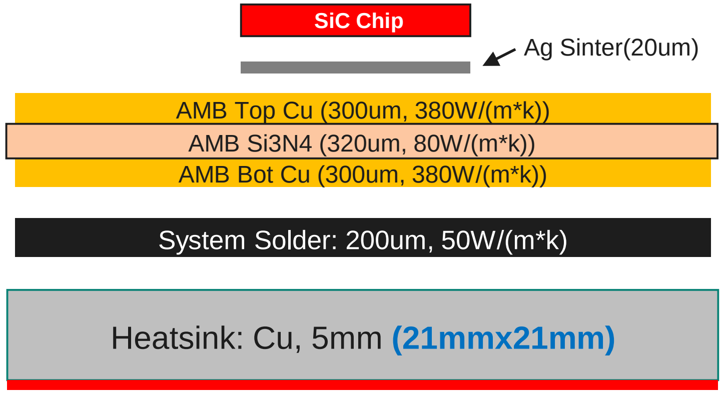
RthJW Results of Embedding PCB Solution VS Module Solution
Case 0 (not compared in the paper) → Rth(j-w) Results



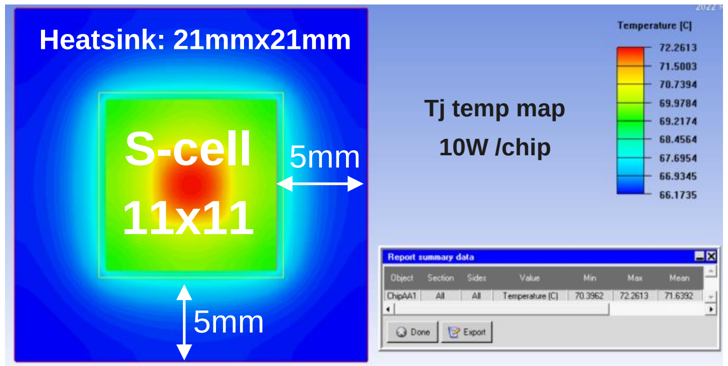
HTC=20000 W/(m²K) and 65C

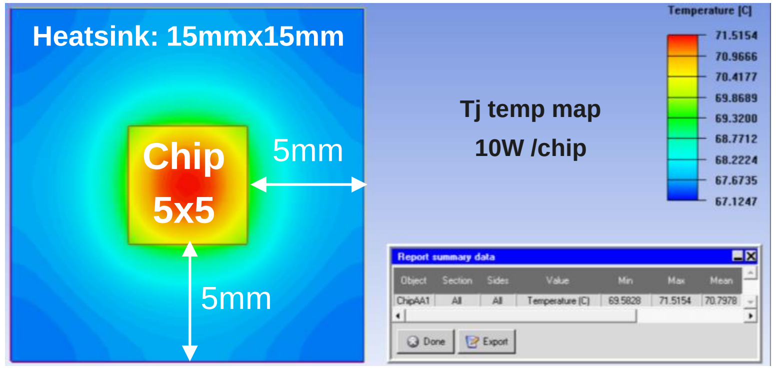


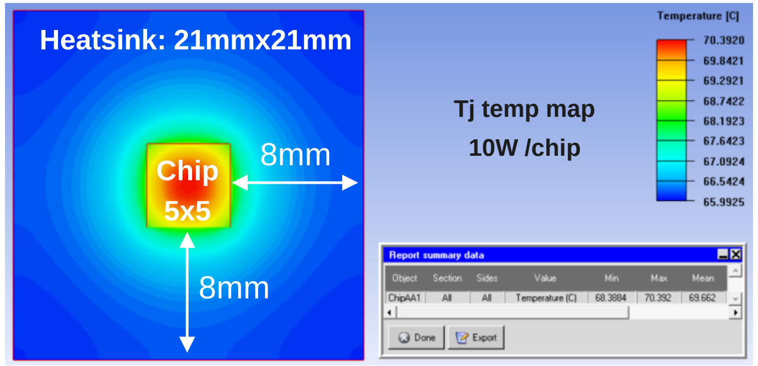
HTC=20000 W/(m²K) and 65C



HTC=20000 W/(m²K) and 65C







- **Tj(avg)=71.6C**
- **Rth(j-w)=(71.6-65)/10W=0.66K/W**

0.66K/W(100%)

- **Tj(avg)=70.80C**
- **Rth(j-w)=(70.80-65)/10W=0.58K/W**

0.58K/W(88%)

- **Tj(avg)=69.66C**
- **Rth(j-w)=(69.66-65)/10W=0.47K/W**

0.47K/W(71%)

Thermal Model of Embedding PCB Solution VS Module Solution
Case 1 (B2 Level) → Setup

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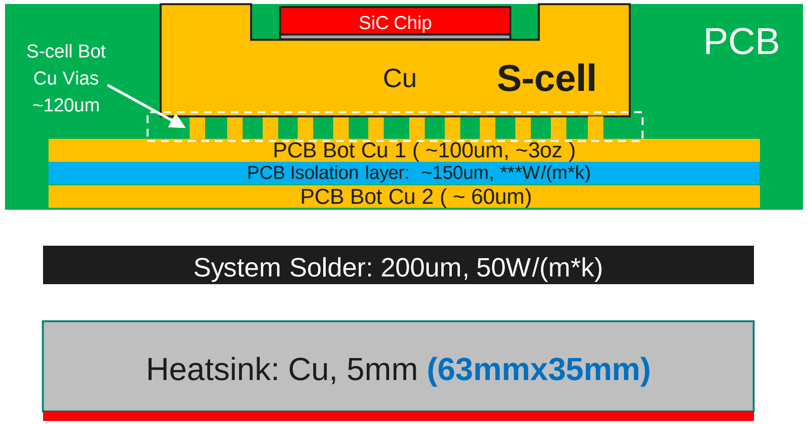
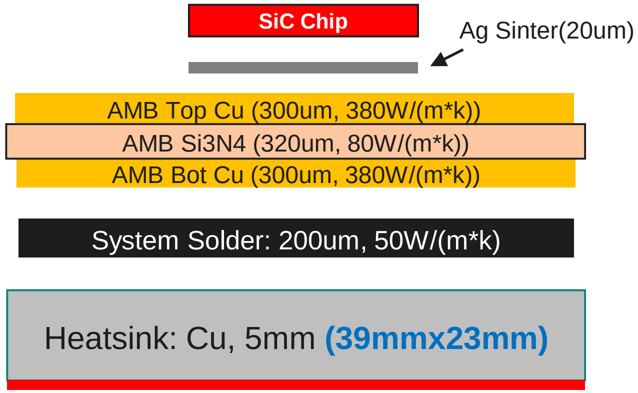
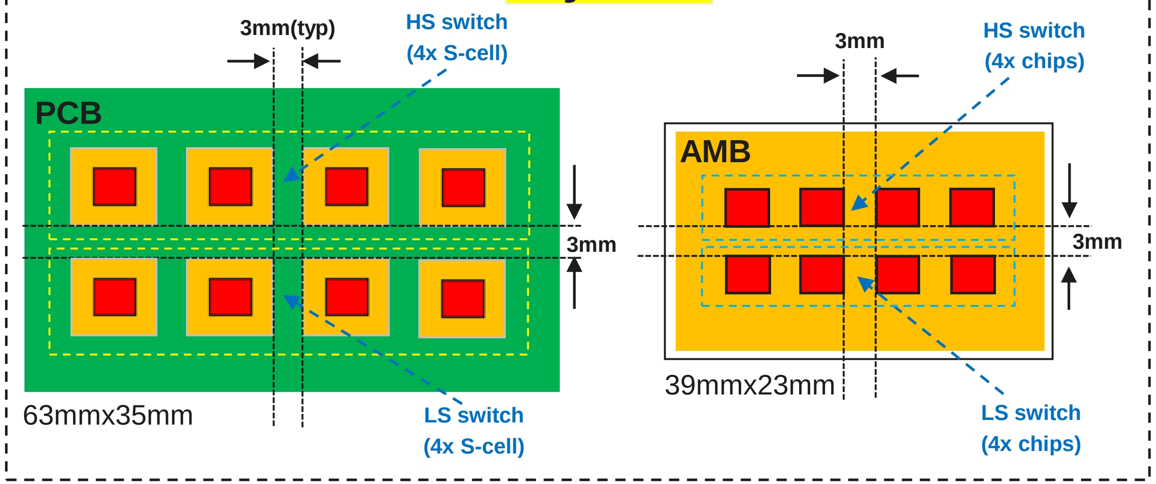


HTC=20000 W/(m²K) and 65C

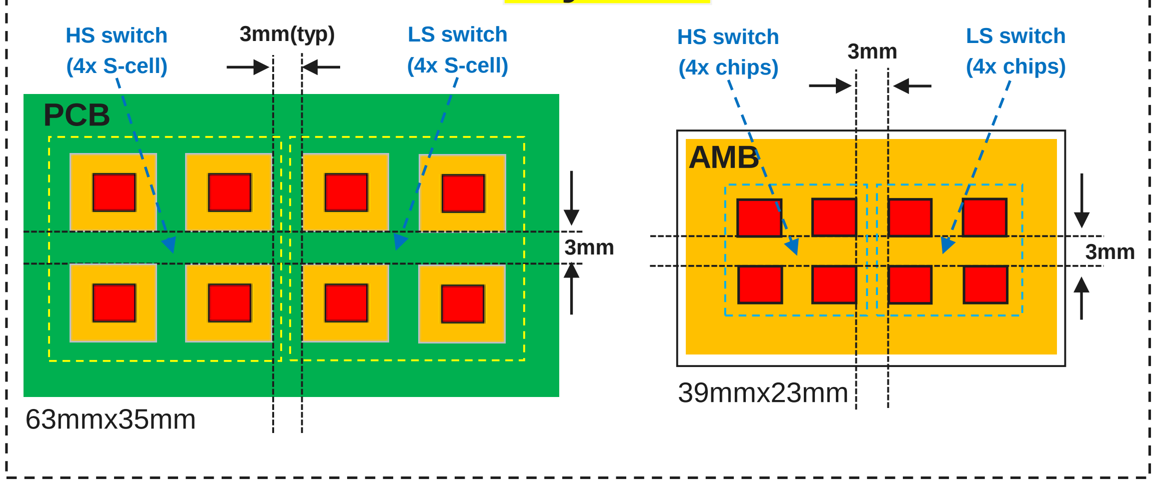


HTC=20000 W/(m²K) and 65C

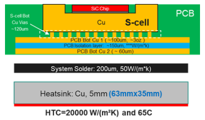
Layout-X

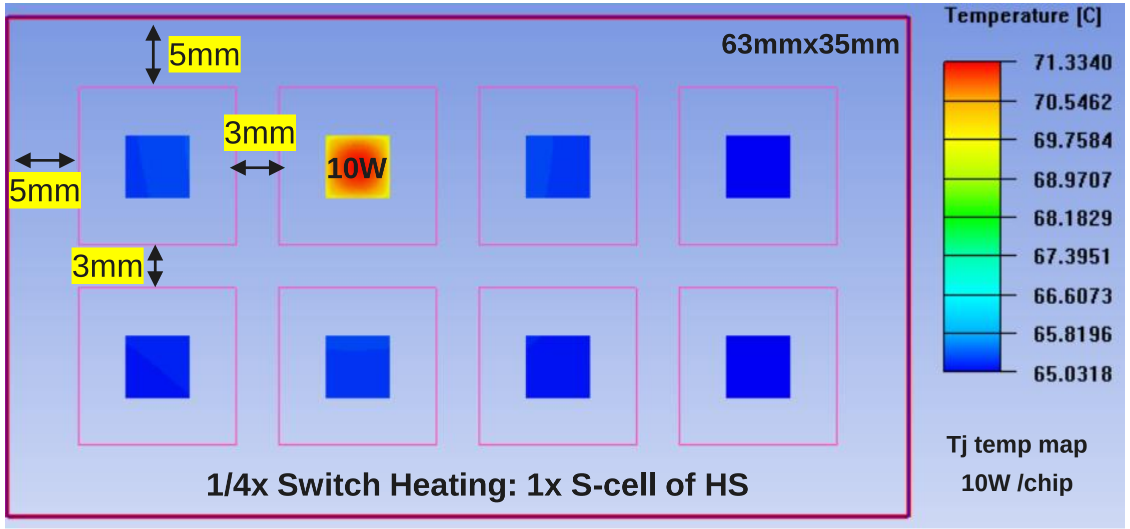


Layout-Y

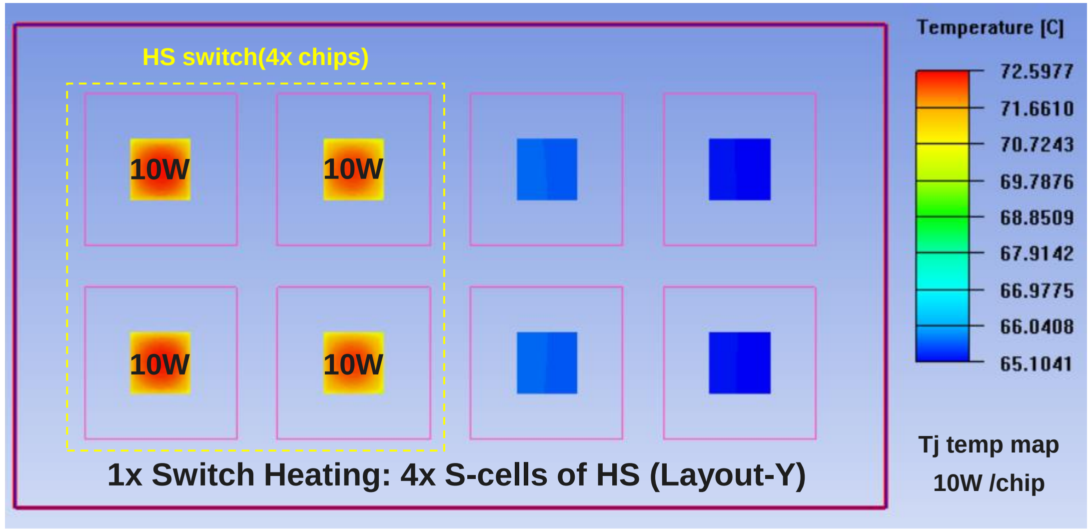


RthJW Results of Embedding PCB Solution VS Module Solution
Case 1 (B2 Level) → Embedding PCB Solution Results

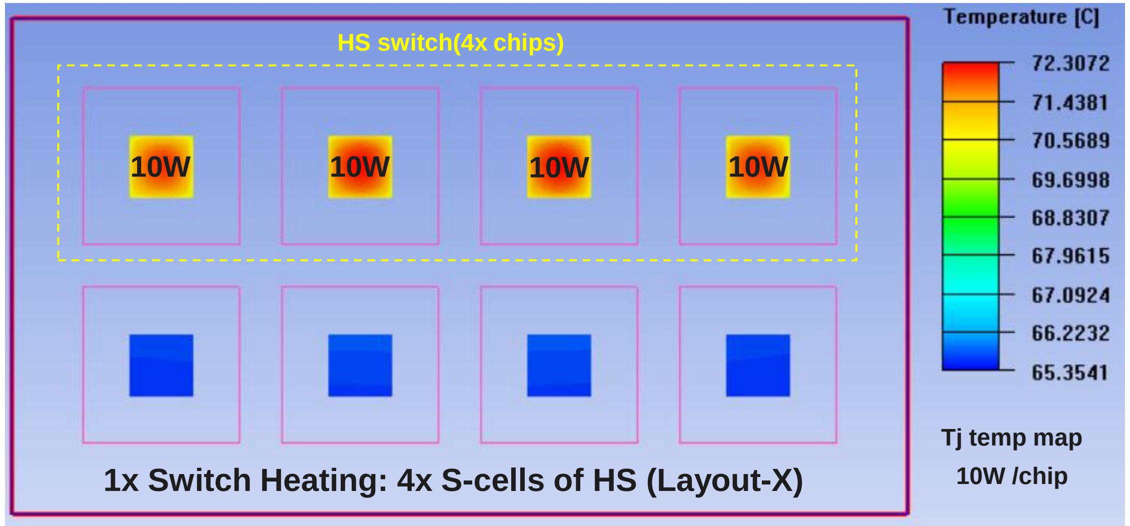




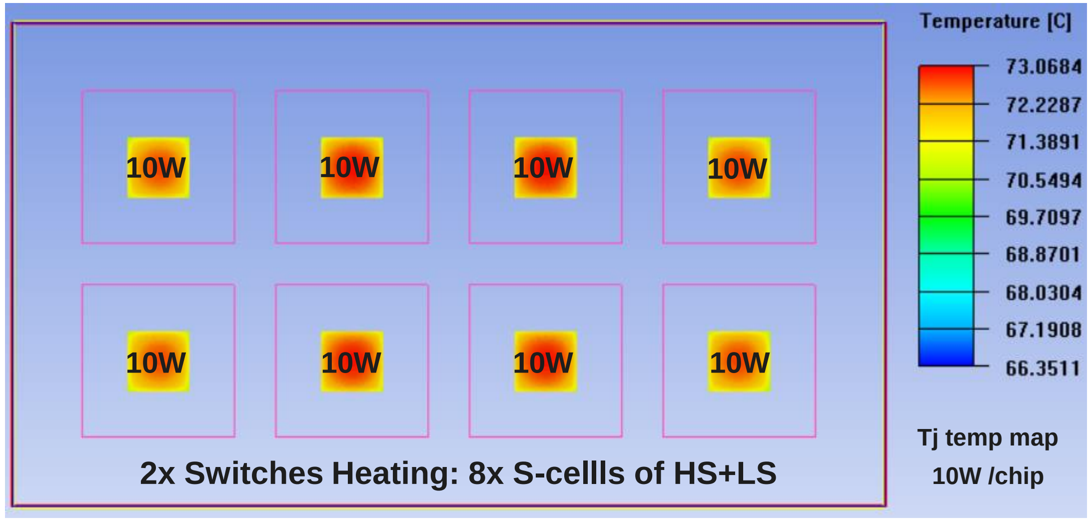
1/4x Switch Heating: 1x S-cell of HS



1x Switch Heating: 4x S-cells of HS (Layout-Y)



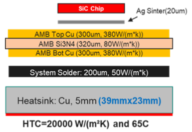
1x Switch Heating: 4x S-cells of HS (Layout-X)

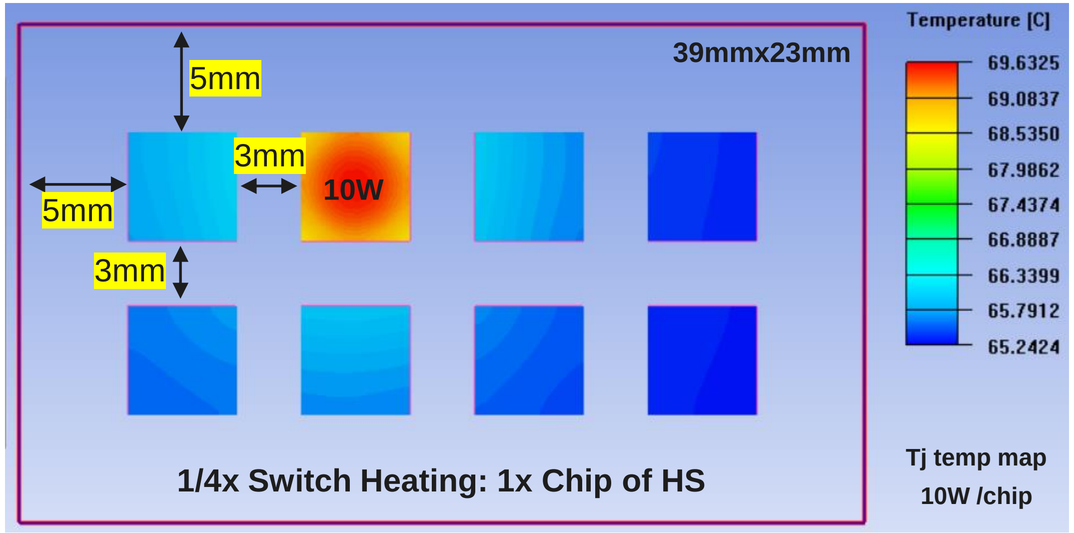


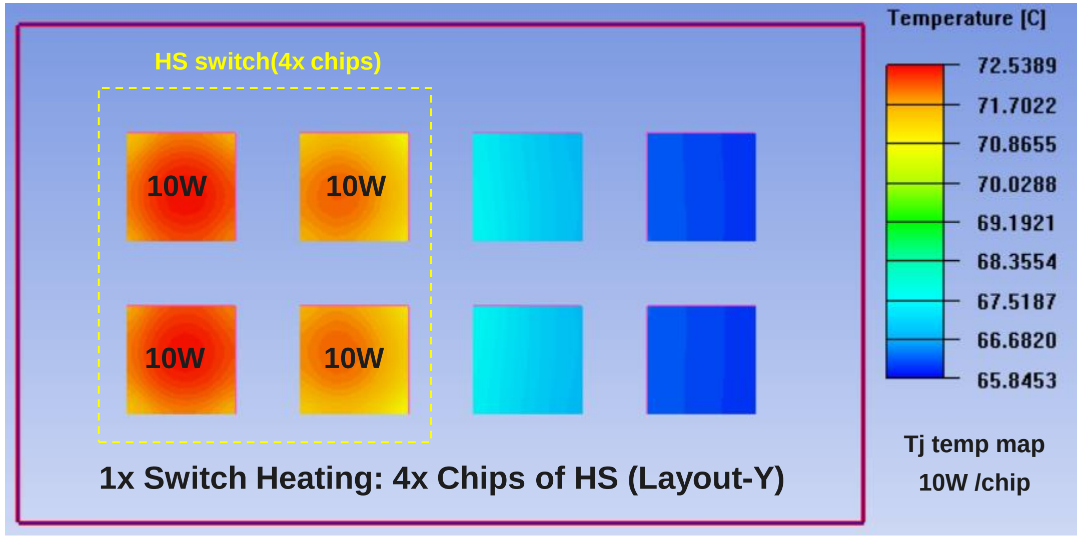
2x Switches Heating: 8x S-cellls of HS+LS

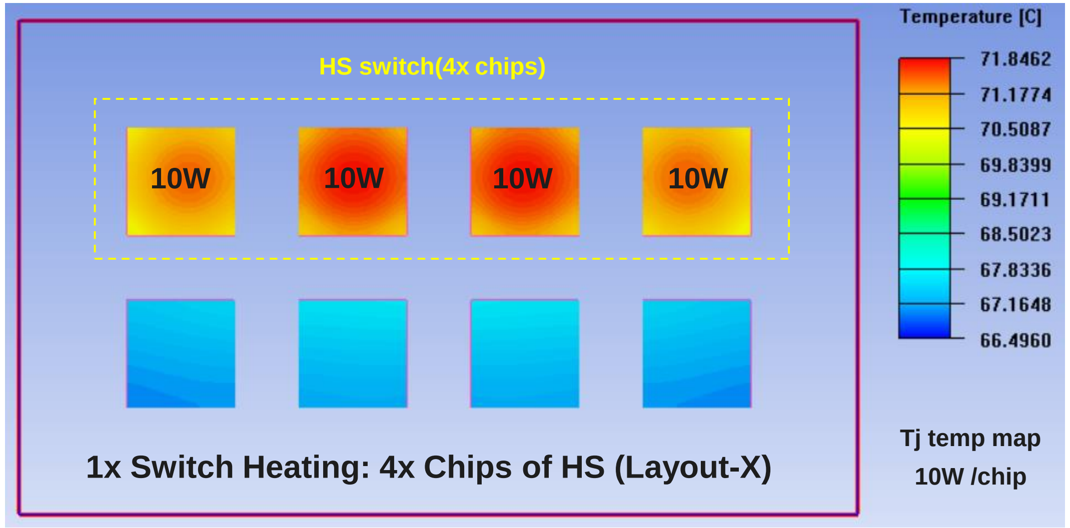
RthJW Results of Embedding PCB Solution VS Module Solution

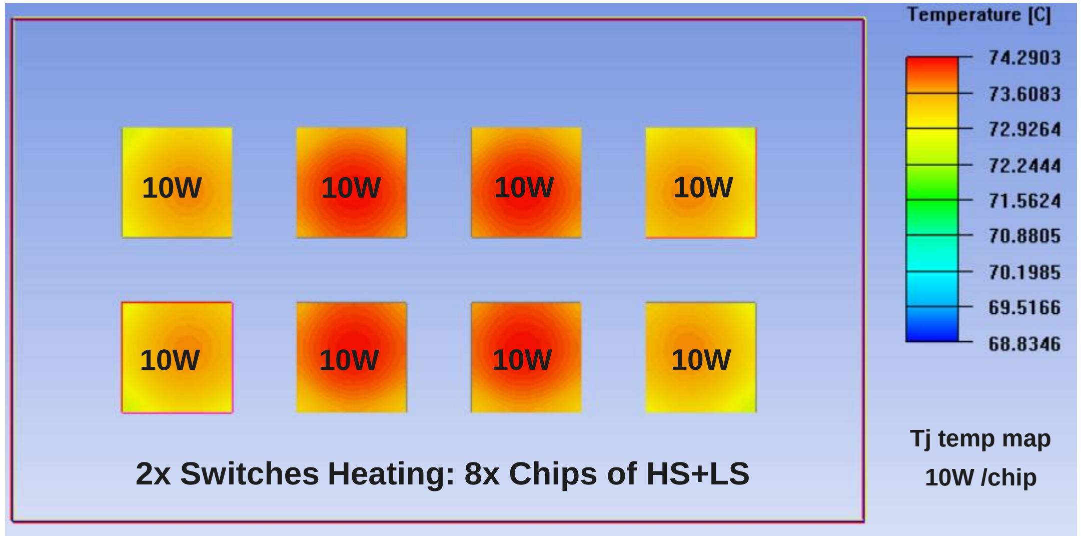
Case 1 (B2 Level) → Module Solution Results











RthJW Results of Embedding PCB Solution VS Module Solution
Case 1 (B2 Level) → RthJW(Normalized) at Layout-X, Layout-Y

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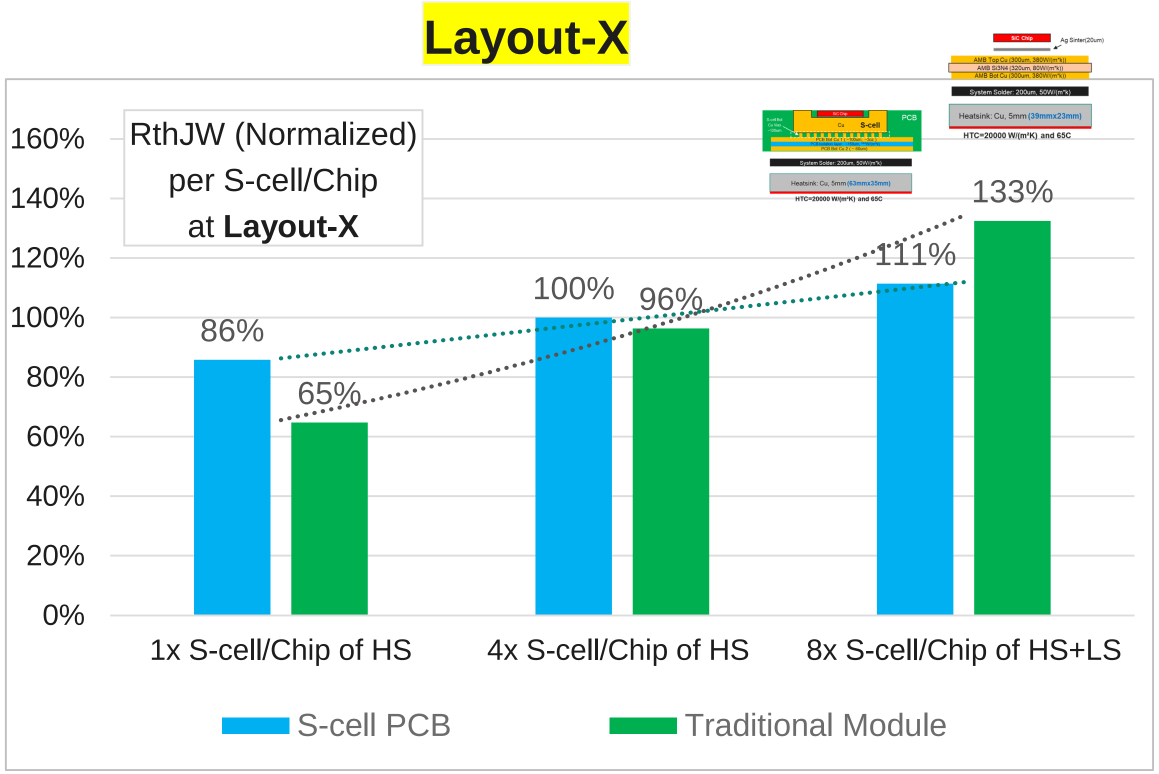

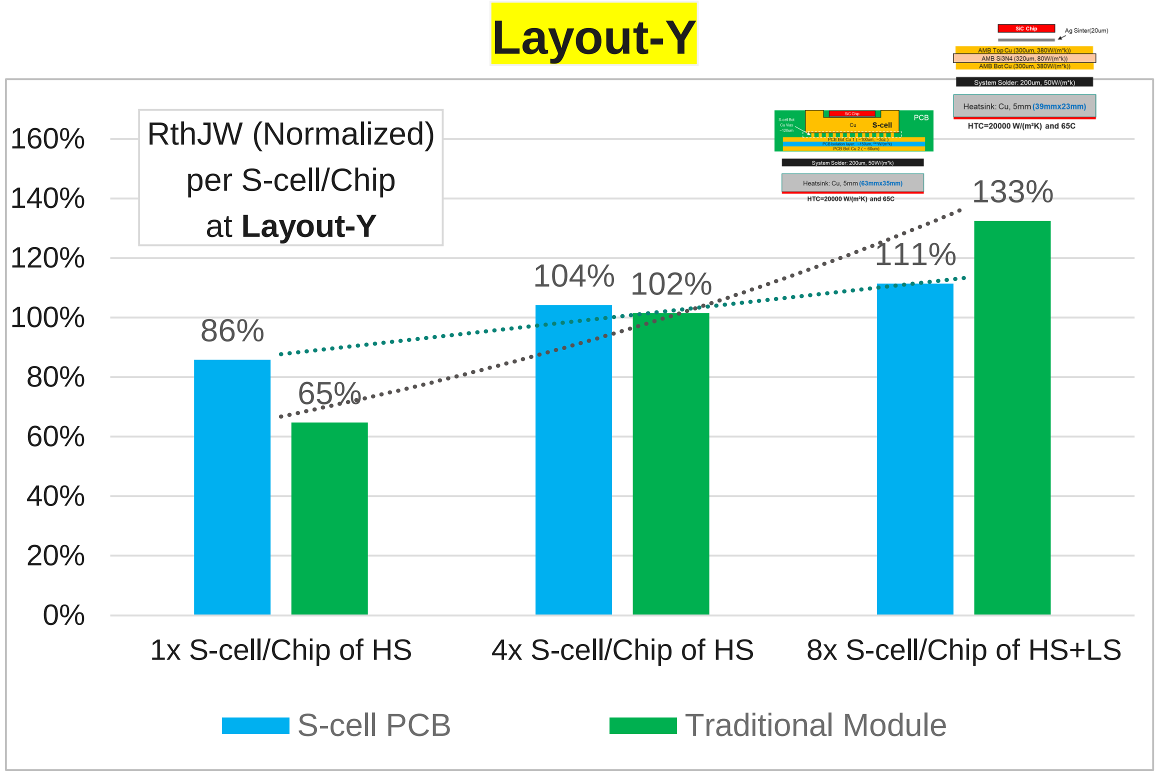

- RthJW per chip: S-cell is higher… **(~20% higher)**
- RthJW per Switch w/o thermal coupling (4xChips): S-cell is similar **(2~4% higher)**
- RthJW per Switch with thermal coupling (8xChips): S-cell is lower **(20%+ lower)**

Close to Application

ZthJW Results of Embedding PCB Solution VS Module Solution
Case 1 (B2 Level) → Results (Normalized) at Layout-X

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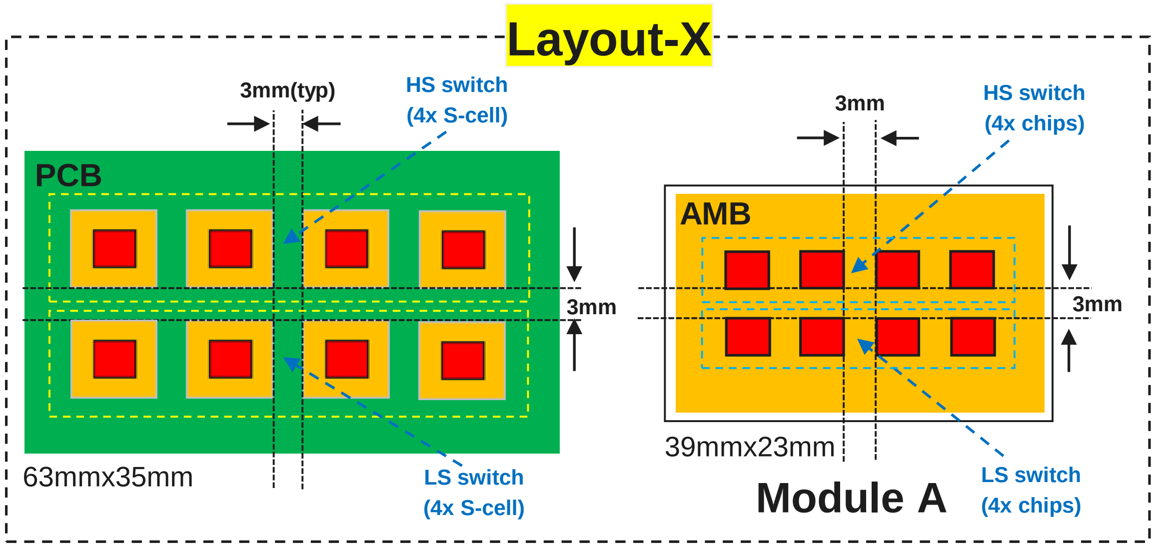
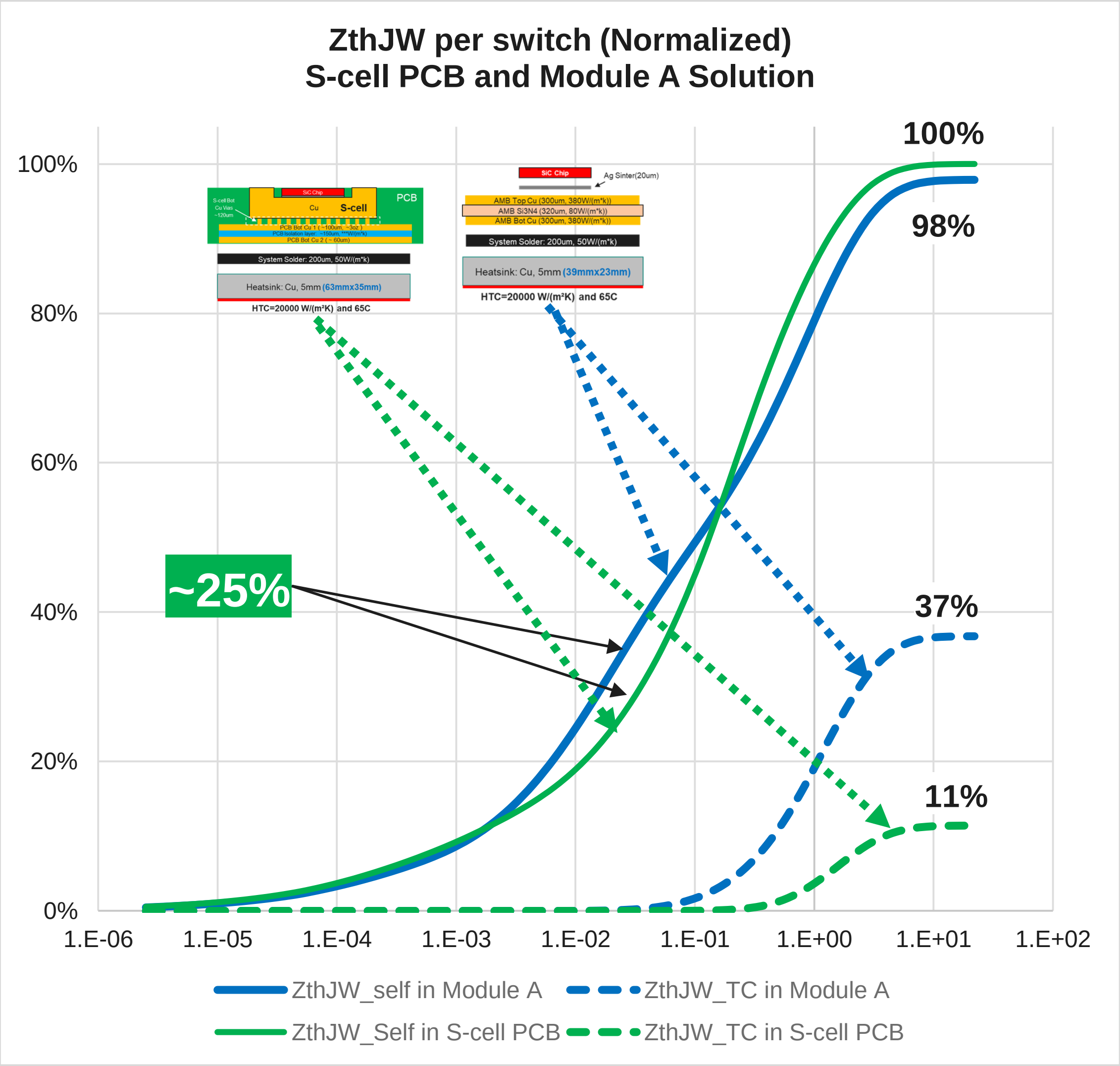
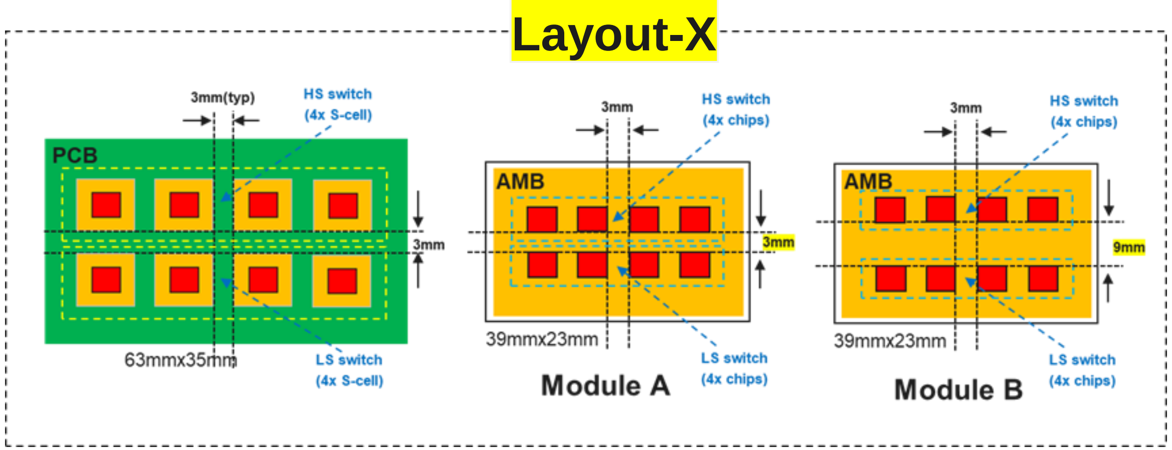


Per switch 4x S-cell/Chip	S-cell PCB	Module A (3mm)
RthJW_Self	100%	98%
RthJW_TC	11%	37%
RthJW_All	111%	135%



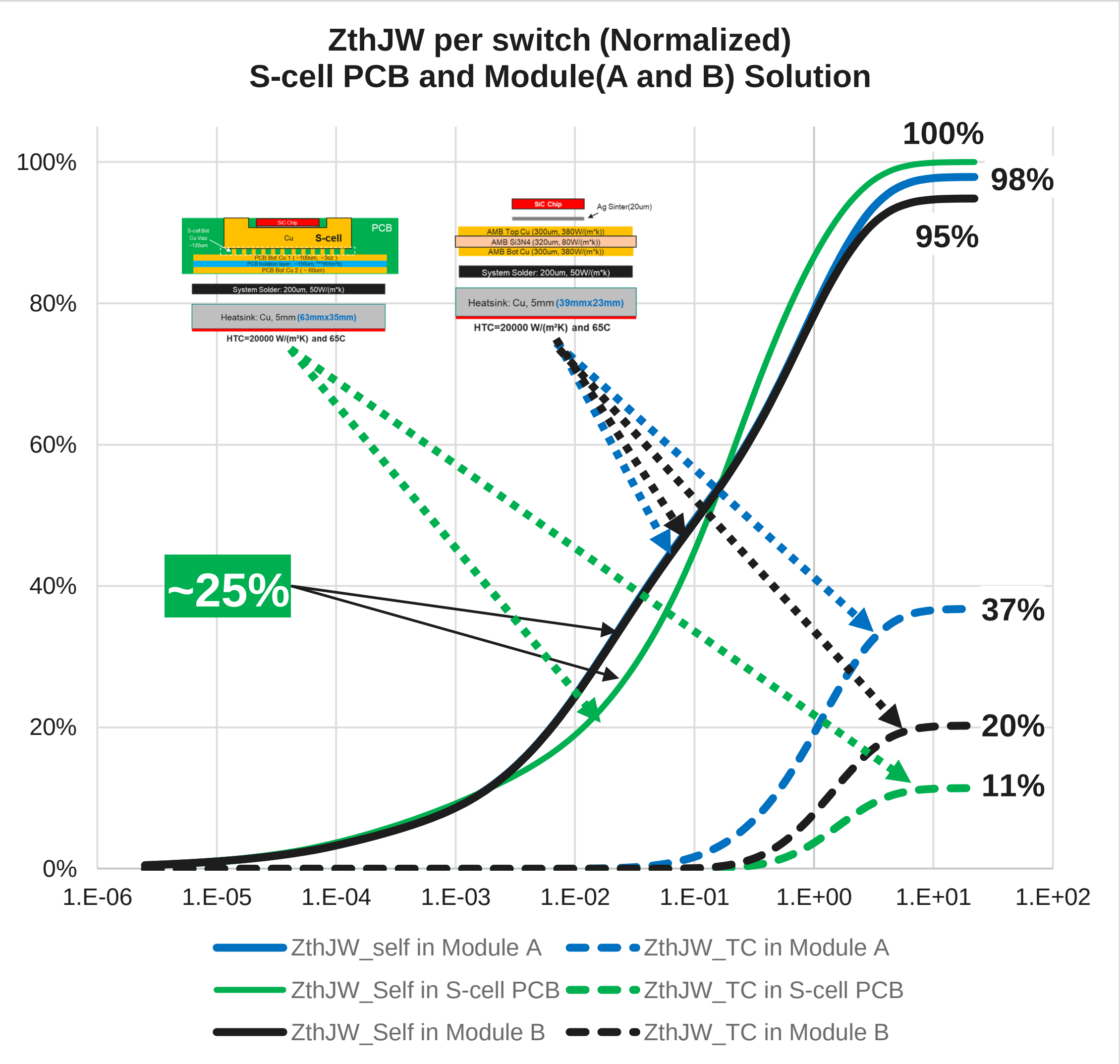
ZthJW Results of Embedding PCB Solution VS Module Solution
Case 1 (B2 Level) → Module B Results (Normalized) at Layout-X



Per switch 4x S-cell/Chip	S-cell PCB	Module A (3mm)	Module B (9mm)
RthJW_Self	100%	98%	95%
RthJW_TC	11%	37%	20%
RthJW_All	111%	135%	115%

+21%

+4%



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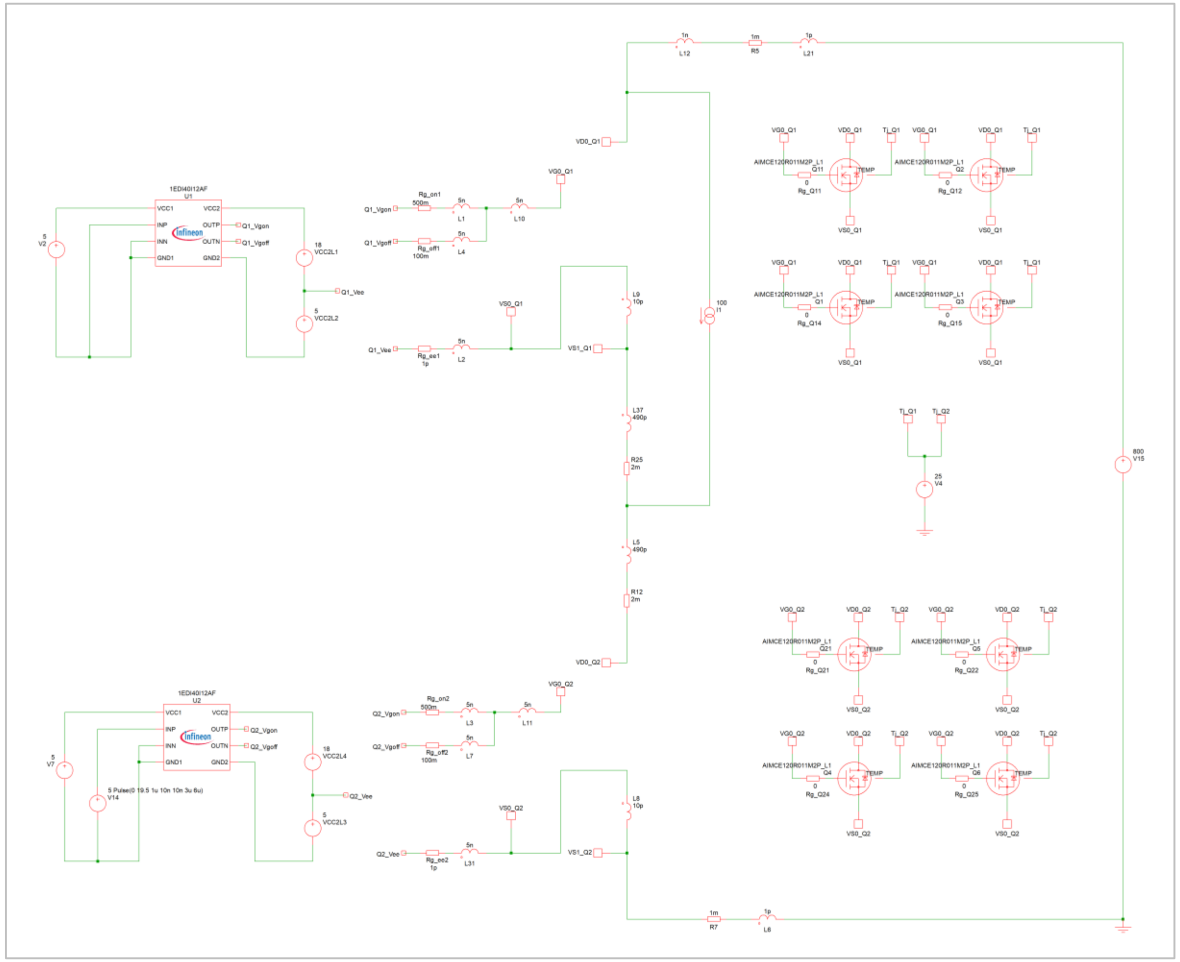
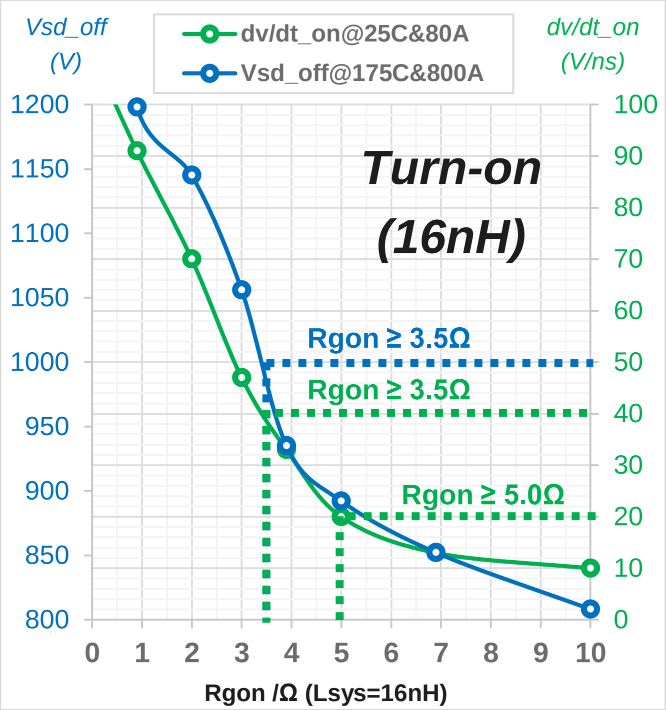
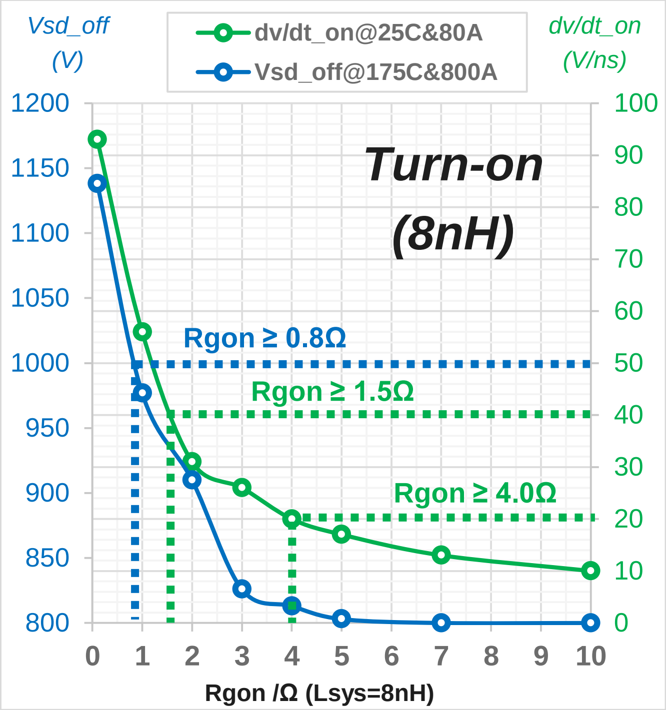
SPICE Simulation Setup

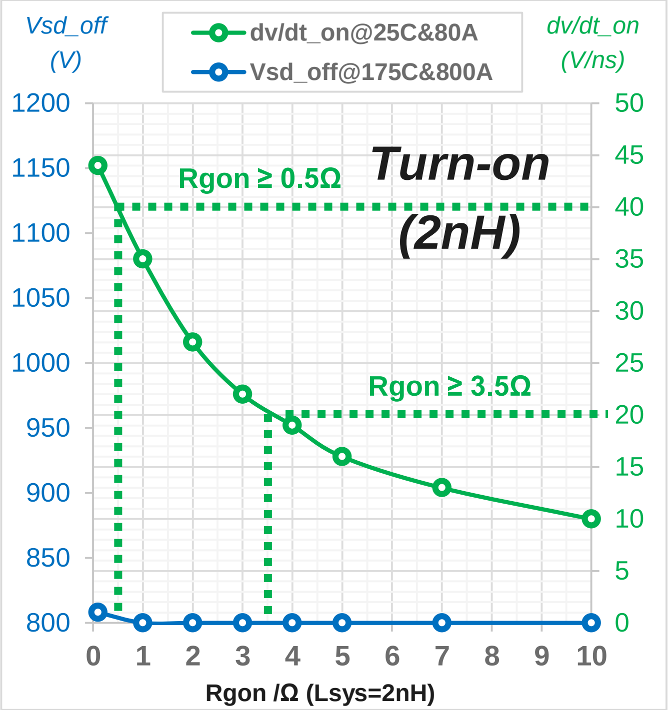
SPICE SIM	Simulation Conditions
Switch	4x S-cell(1200V/25mm2)
Vdc	800V
Lsys	2nH, 8nH, 16nH
Ids	0~800A
Vgs	18V/-5V
Tvj	25C, 175C
Rg Selection	1) Vds_peak ≤ 1000V & dv/dt ≤ 20kV/us
	2) Vds_peak ≤ 1000V & dv/dt ≤ 40kV/us



SPICE Simulation
Rgon Selection







Rgon	Vsd_off	dv/dt_on		Vsd_off ≤ 1000V	
	≤ 1000V	≤ 20kV/s	≤ 40kV/s	≤ 20kV/s	≤ 40kV/s
16nH	≥ 3.5Ω	≥ 5.0Ω	≥ 3.5Ω	≥ 5.0Ω	≥ 3.5Ω (40kV/s)
8nH	≥ 0.8Ω	≥ 4.0Ω	≥ 1.5Ω	≥ 4.0Ω	≥ 1.5Ω (40kV/s)
2nH	≥ 0.1Ω	≥ 3.5Ω	≥ 0.5Ω	≥ 3.5Ω	≥ 0.5Ω (40kV/s)

SPICE Simulation
Rgoff Selection

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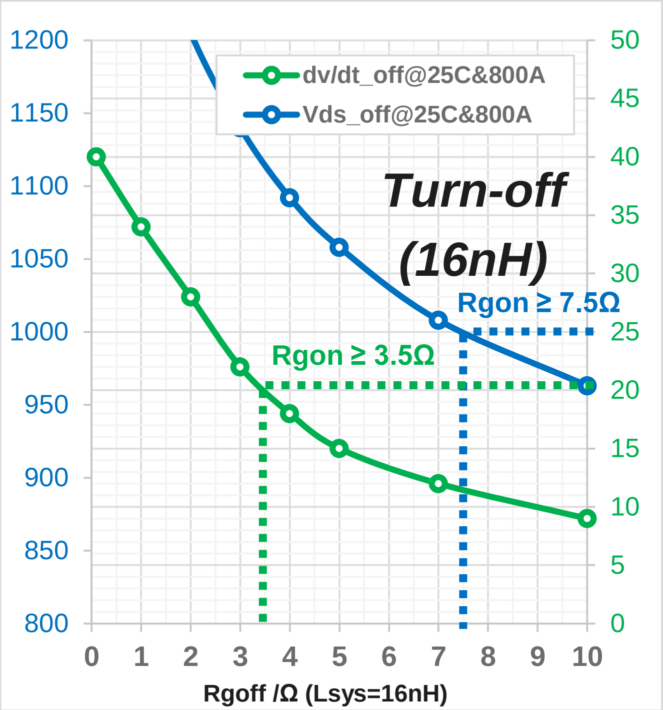
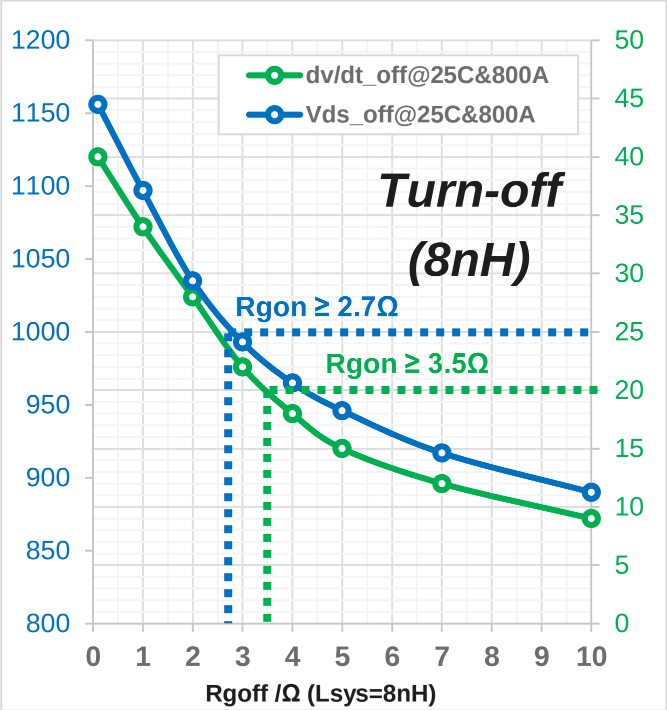
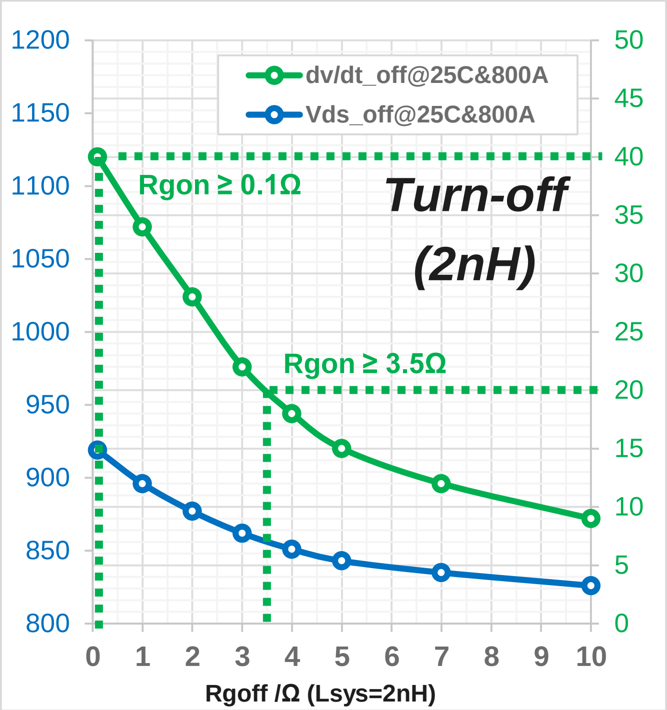






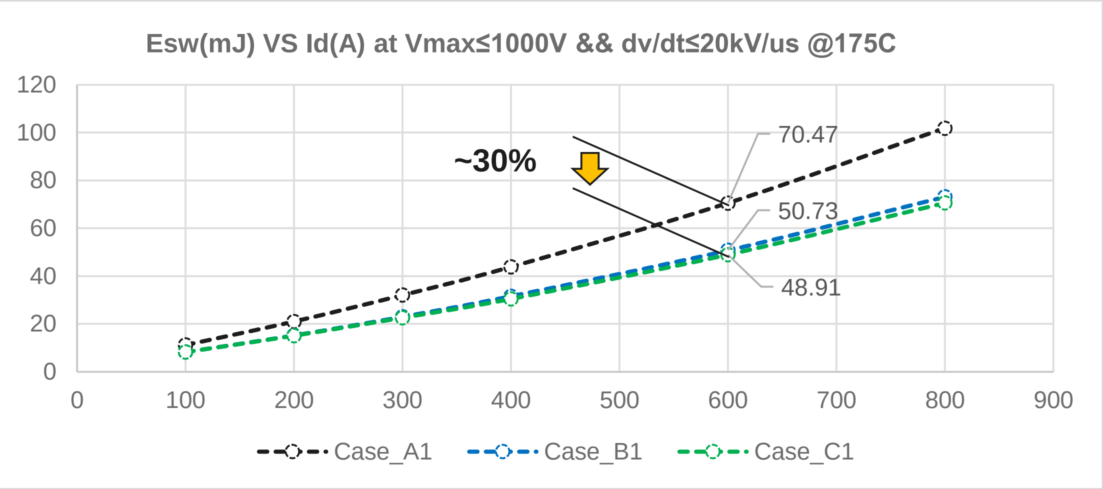
Rgoff	Vds_off	dv/dt_off		Vds_off ≤ 1000V	
	≤ 1000V	≤ 20kV/s	≤ 40kV/s	≤ 20kV/s	≤ 40kV/s
16nH	≥ 7.5Ω	≥ 3.5Ω	≥ 0.1Ω	≥ 7.5Ω	≥ 7.5Ω (25kV/s)
8nH	≥ 2.7Ω	≥ 3.5Ω	≥ 0.1Ω	≥ 3.5Ω	≥ 2.7Ω (25kV/s)
2nH	≥ 0.1Ω	≥ 3.5Ω	≥ 0.1Ω	≥ 3.5Ω	≥ 0.1Ω (40kV/s)

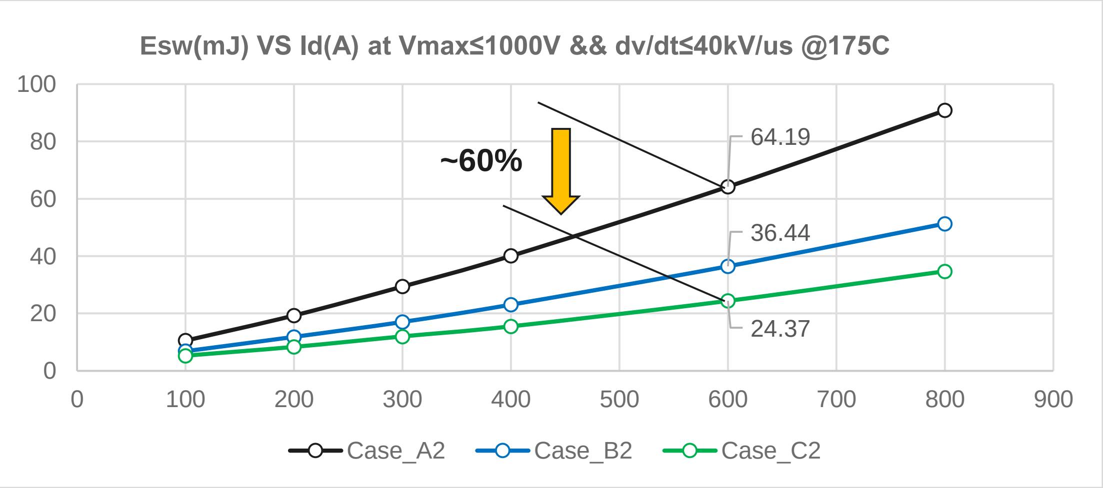
SPICE Simulation
Esw SIM by SPICE model

Rgon	Vsd_off	dv/dt_on		Vsd_off ≤ 1000V	
	≤ 1000V	≤ 20kV/us	≤ 40kV/us	≤ 20kV/us	≤ 40kV/us
16nH	≥ 3.5Ω	≥ 5.0Ω	≥ 3.5Ω	≥ 5.0Ω	≥ 3.5Ω
8nH	≥ 0.8Ω	≥ 4.0Ω	≥ 1.5Ω	≥ 4.0Ω	≥ 1.5Ω
2nH	≥ 0.1Ω	≥ 3.5Ω	≥ 0.5Ω	≥ 3.5Ω	≥ 0.5Ω

Rgoff	Vds_off	dv/dt_off		Vds_off ≤ 1000V	
	≤ 1000V	≤ 20kV/us	≤ 40kV/us	≤ 20kV/us	≤ 40kV/us
16nH	≥ 7.5Ω	≥ 3.5Ω	≥ 0.1Ω	≥ 7.5Ω	≥ 7.5Ω
8nH	≥ 2.7Ω	≥ 3.5Ω	≥ 0.1Ω	≥ 3.5Ω	≥ 2.7Ω
2nH	≥ 0.1Ω	≥ 3.5Ω	≥ 0.1Ω	≥ 3.5Ω	≥ 0.1Ω

Vmax ≤ 1000V && dv/dt ≤ 20kV/us	Case A1 Lsys=16nH Rgon=5.0Ω Rgoff=7.5Ω	Case B1 Lsys=8nH Rgon=4.0Ω Rgoff=3.5Ω	Case C1 Lsys=2nH Rgon=3.5Ω Rgoff=3.5Ω
Vmax ≤ 1000V && dv/dt ≤ 40kV/us	Case A2 Lsys=16nH Rgon=3.5Ω Rgoff=7.5Ω	Case B2 Lsys=8nH Rgon=1.5Ω Rgoff=2.7Ω	Case C2 Lsys=2nH Rgon=0.5Ω Rgoff=0.1Ω





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The xEV inverter system analysis
Simulation Setup → RthJW and Esw and System Conditions

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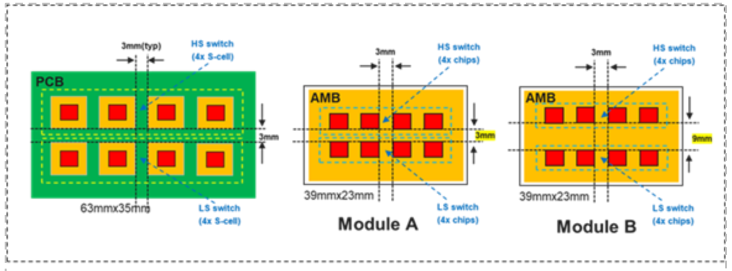
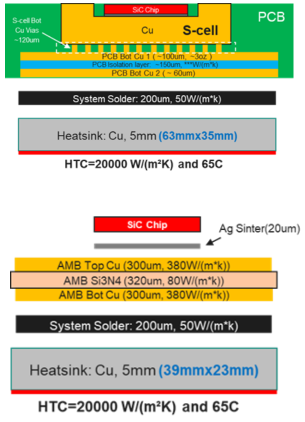
Supposed RthJW for simulation setup



Per switch 4x S-cell/Chip	S-cell PCB	Module A (3mm)	Module B (9mm)
RthJW_Self	100%	98%	95%
RthJW_TC	11%	37%	20%
RthJW_All	111%	135%	115%

+21%

+4%



Same Ratio

Per switch 4x S-cell/Chips	S-cell PCB	Module A (3mm)	Module B (9mm)
RthJW_Self	0.150	0.148	0.143
RthJW_TC	0.017	0.055	0.031
RthJW_All	0.167	0.202	0.174

Supposed Esw for simulation setup

Reuse the Esw data by SPICE simulation

Supposed System Simulation Conditions

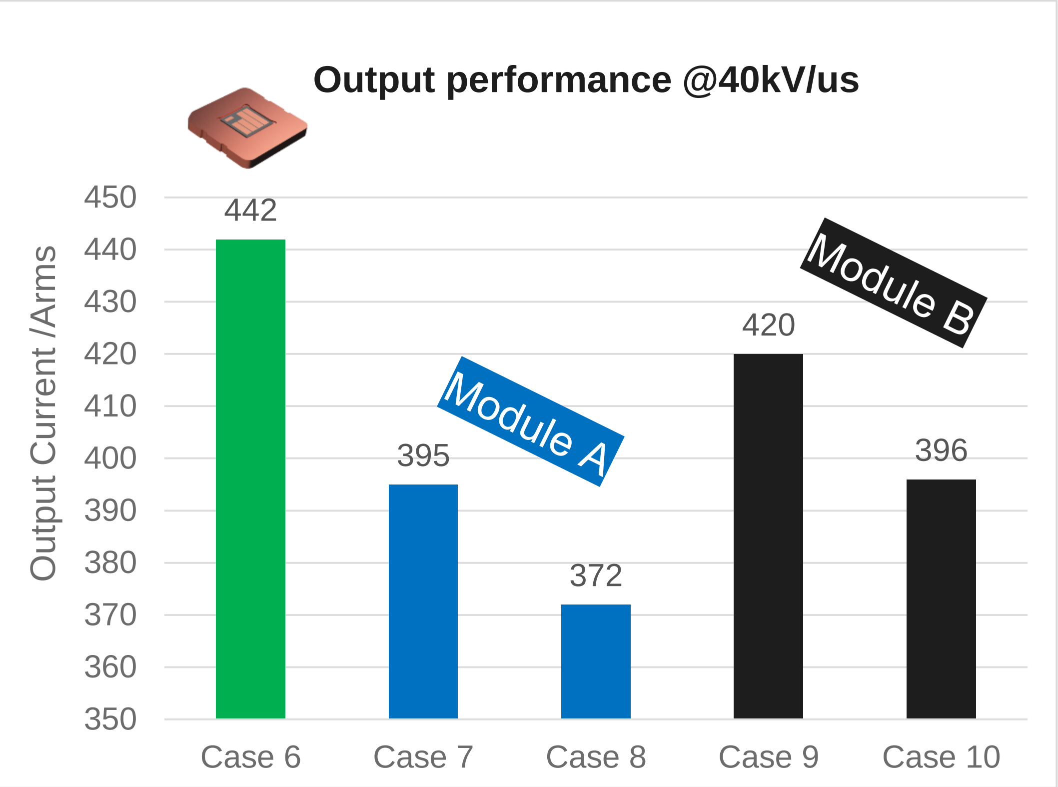
PLECS SIM	Simulation Conditions
per Switch	4x S-cell/Chips
Vdc	800V
fsw	8kHz
fout	400Hz
Cos_phi	0.9
Modi	1.0
Tw	65C

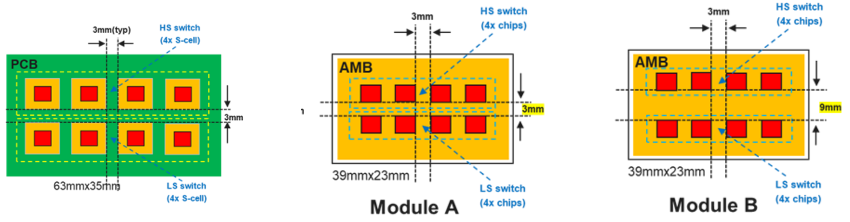
PS: full load is 400Arms+, light load is ~80Arms

The xEV inverter system analysis
Simulation Results Comparison on Max Output Performance

20kV/us	Esw Spec	ZthJF (Self+TC) /K/W	Output @Tvjmax=175C	Pdc /W	Psw /W	Ptot /W
Case 1	2nH_20kV/us	S-cell PCB 0.15*(1+11%)	420Arms (100%)	485	119	604
Case 2	8nH_20kV/us	Module A 0.148*(1+37%)	382Arms	397	111	508
Case 3	16nH_20kV/us		366Arms (-13%)	364	148	512
Case 4	8nH_20kV/us	Module B 0.143*(1+22%)	408Arms (-3%)	454	119	573
Case 5	16nH_20kV/us		392Arms	419	159	578

40kV/us	Esw Spec	ZthJF (Self+TC) /K/W	Output @Tvjmax=175C	Pdc /W	Psw /W	Ptot /W
Case 6	2nH_40kV/us	S-cell PCB 0.15*(1+11%)	442Arms (100%)	540	64	604
Case 7	8nH_40kV/us	Module A 0.148*(1+37%)	395Arms	428	84	512
Case 8	16nH_40kV/us		372Arms (-16%)	378	138	516
Case 9	8nH_40kV/us	Module B 0.143*(1+22%)	420Arms (-5%)	482	90	572
Case 10	16nH_40kV/us		396Arms	427	151	578

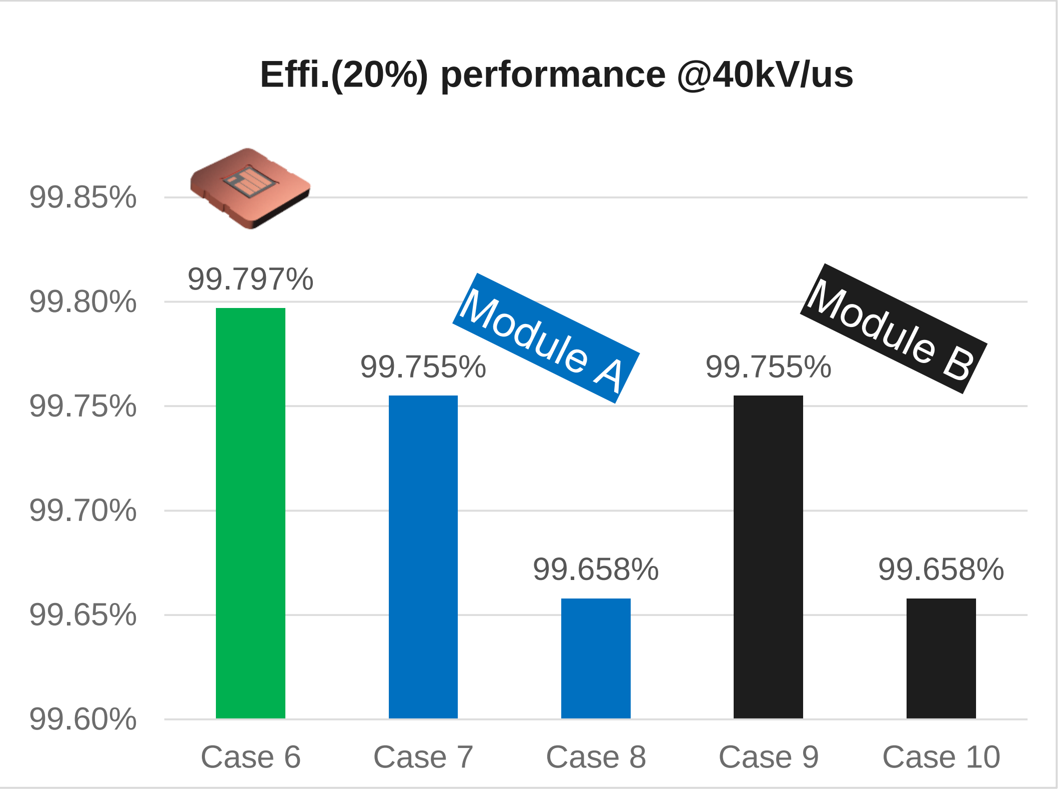


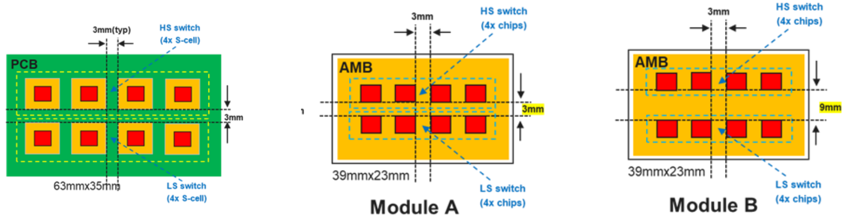


The xEV inverter system analysis
Simulation Results Comparison on light load Effi.

20kV/us	Esw Spec	ZthJF (Self+TC) /K/W	Effi @80Arms	Pdc /W	Psw /W	Ptot /W
Case 1	2nH_20kV/us	S-cell PCB 0.15*(1+11%)	99.72%	10	18	28
Case 2	8nH_20kV/us	Module A 0.148*(1+37%)	99.72%	10	19	29
Case 3	16nH_20kV/us		99.64%	10	27	37
Case 4	8nH_20kV/us	Module B 0.143*(1+22%)	99.72%	10	19	29
Case 5	16nH_20kV/us		99.64%	10	27	37

40kV/us	Esw Spec	ZthJF (Self+TC) /K/W	Effi @80Arms	Pdc /W	Psw /W	Ptot /W
Case 6	2nH_40kV/us	S-cell PCB 0.15*(1+11%)	99.797%	10	11	22
Case 7	8nH_40kV/us	Module A 0.148*(1+37%)	99.755%	10	15	25
Case 8	16nH_40kV/us		99.658%	10	25	35
Case 9	8nH_40kV/us	Module B 0.143*(1+22%)	99.755%	10	15	25
Case 10	16nH_40kV/us		99.658%	10	25	35





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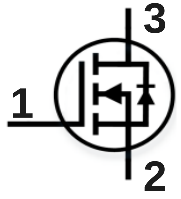
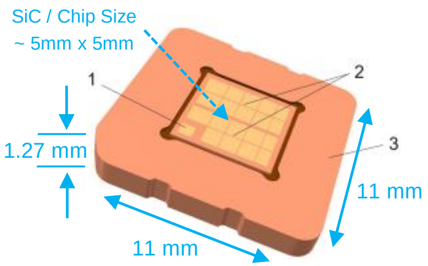
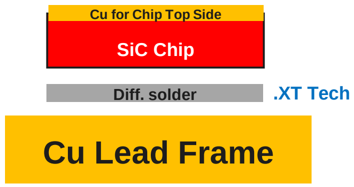
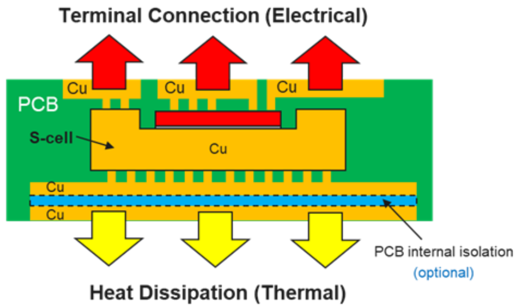
Conclusion

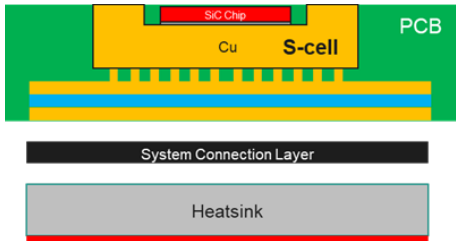
- One Innovative SiC chip Embedding PCB solution was introduced
- the Advantages of S-cell based embedding PCB solution
  - Lower Thermal performance (SIM by FEM thermal simulation): **4~21% lower**
  - Lower Switching losses (SIM by SPICE simulation): **4~60% lower**
  - Inverter level (SIM by PLECS simulation): **higher output (3%~16%) and light-load effi.(0.08%~0.14%)**











One Innovative SiC chip Embedding PCB solution based on Infineon S-cell Product

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