



UNIVERSITY OF
CAMBRIDGE

Ultra-Compact and Efficient Power Supply Enabling AI Computing

Prof Teng Long

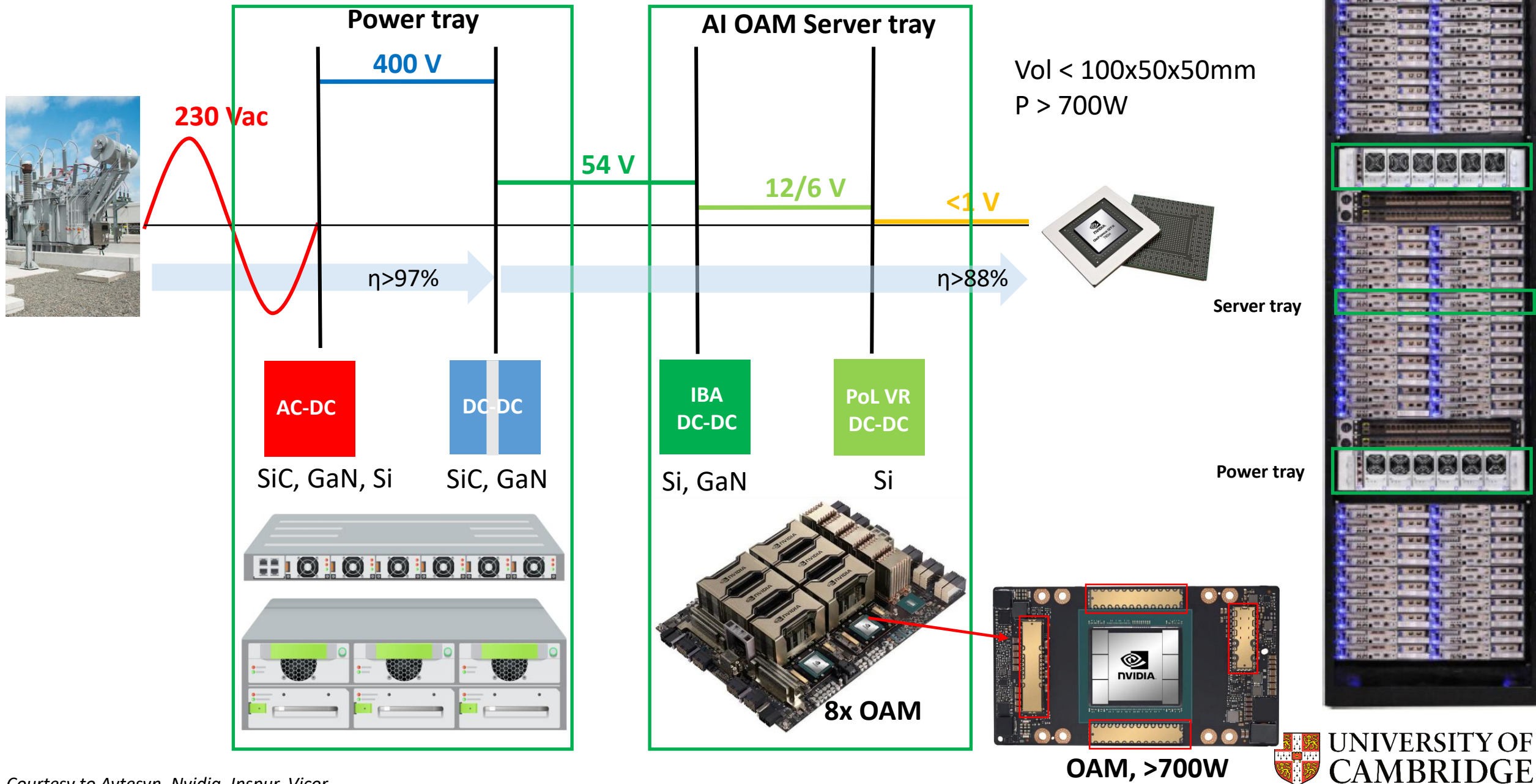
Contents

- State-of-the-art Power Supply Architecture for AI datacentres
- Advanced Power Electronics Packaging for for High Integration
- Smart Soft-Switching using Electroluminescence

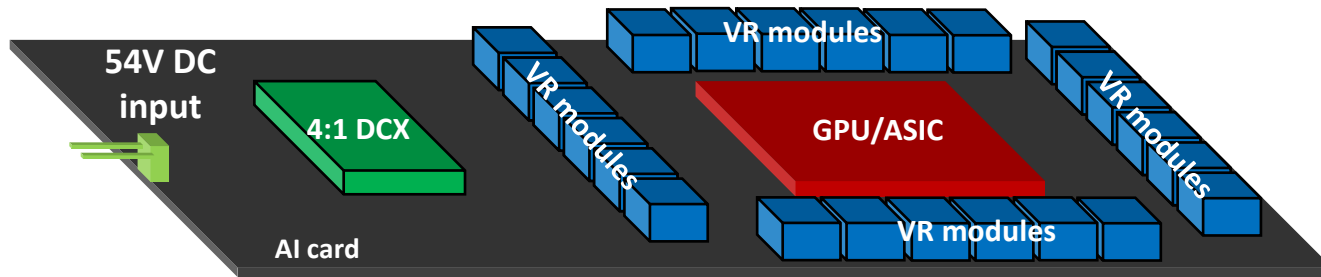
Contents

- State-of-the-art Power Supply Architecture for AI datacentres
- Advanced Power Electronics Packaging for for High Integration
- Smart Soft-Switching using Electroluminescence

Power supply architecture for AI servers

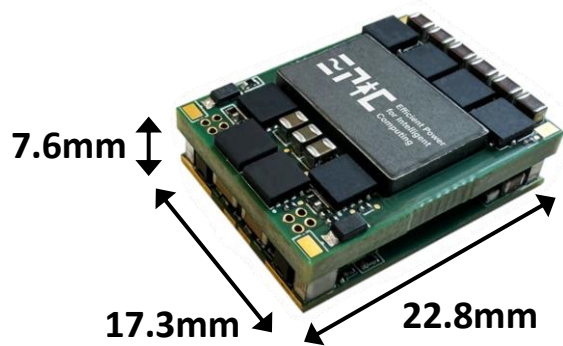


Lateral Two-Stage Architecture: DCX 4:1 → VR



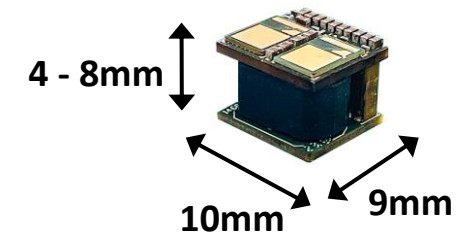
Stage 1: Fixed-Ratio DC transformer (DCX)

- ❑ Fixed ratio voltage conversion, X:1 transfer DC voltage like a transformer (DCX)
- ❑ 4:1 DCX input 40-60V, output 10-15V, typical size: 23mm x 17mm x 8mm (OCP standardized)
- ❑ 5:1, 6:1, 8:1, 10:1, 48:1 are also available
- ❑ Variants of LLC topologies, non-isolated, ZVS soft-switching for high efficiency.

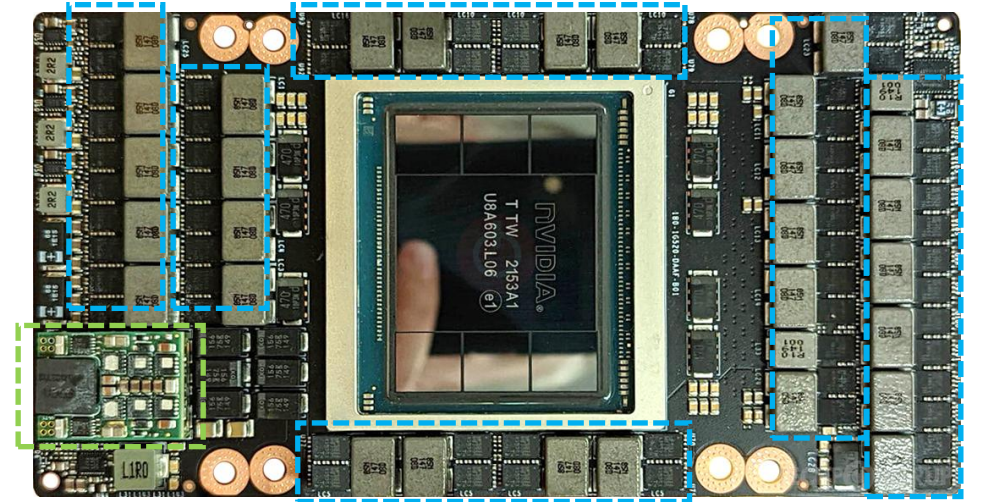


Stage 2: Voltage Regulator (VR)

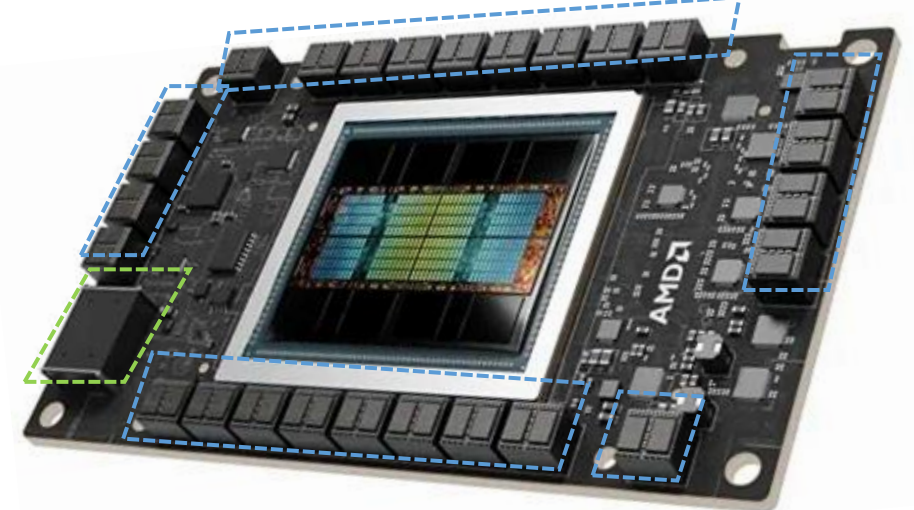
- ❑ High dynamic response requirement: >10A/ns
- ❑ Multi-phase BUCK topology, using coupled or non-coupled inductors
- ❑ DrMOS and multi-phase BUCK controller from the same vendor
- ❑ Trans-Inductor VR (TLVR) BUCK is trending due to better dynamic (but also issues)



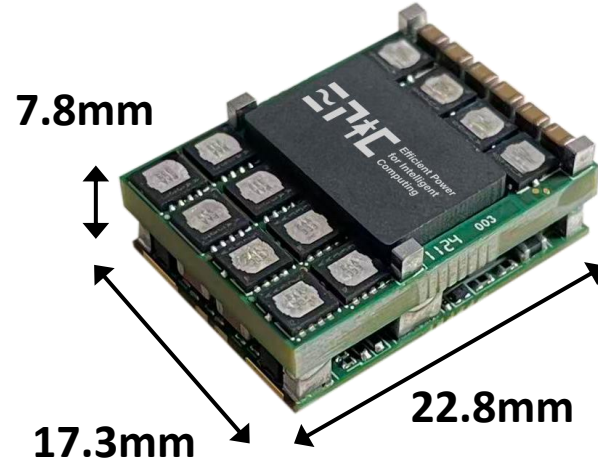
Nvidia H100 AI card



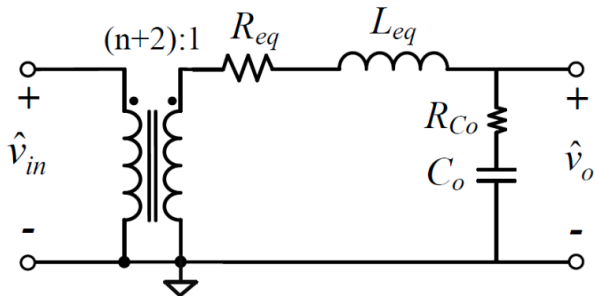
AMD MI300x AI card



Intermediate Bus Converter (fixed-ratio DCX)

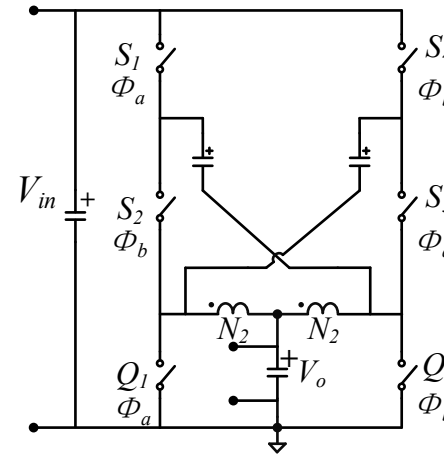


- **1.5kW** high output power
- **98.0%** peak effi and **97.0%** full-load effi.
- **8.1kW/in³** power density
- 1.1% efficiency improvement compared to conventional solutions



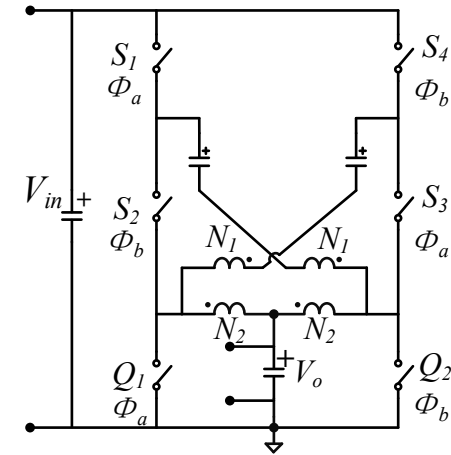
$$L_{eq} = \frac{\pi^2 T_s^2}{4(n+2)^2 T_r^2} L_r$$

$$R_{eq} = \frac{\pi^2 T_s}{8(n+2)^2 T_r} R_{LLC}$$



$$\frac{V_o}{V_{in}} = \frac{1}{4}$$

- Delta topology patent
- Fixed 4: 1
- DC bias on Cr



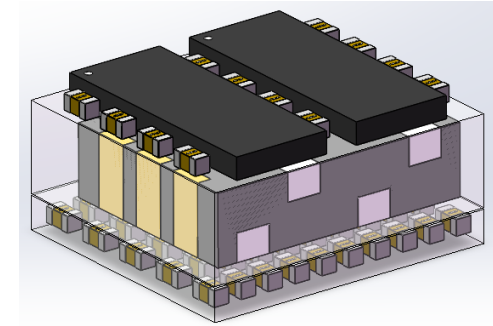
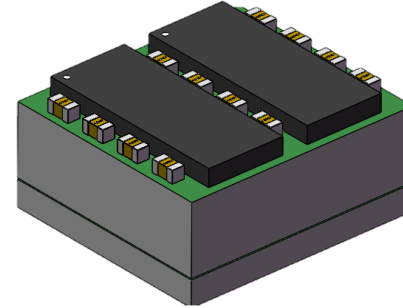
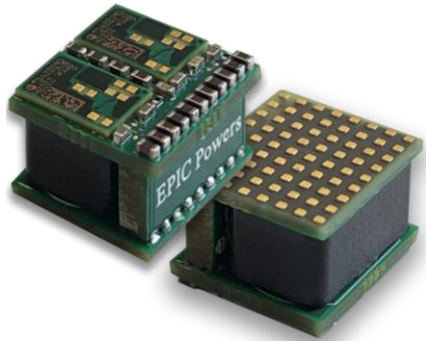
$$\frac{V_o}{V_{in}} = \frac{1}{2(n+2)}$$

- Infineon **HSC** topology patent
- Suitable for 6: 1, 8: 1 etc.
- DC bias on Cr
- Complex current loop



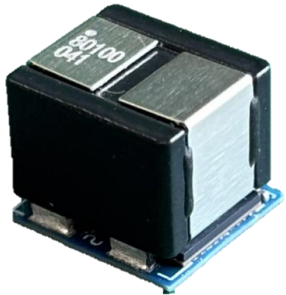
Open-loop LLC variants suits fixed ratio IBA converter

Voltage Regulator (VR) using Buck topology



Top: DrMOS → better cooling

Middle: inductor → low DCR but less coupling



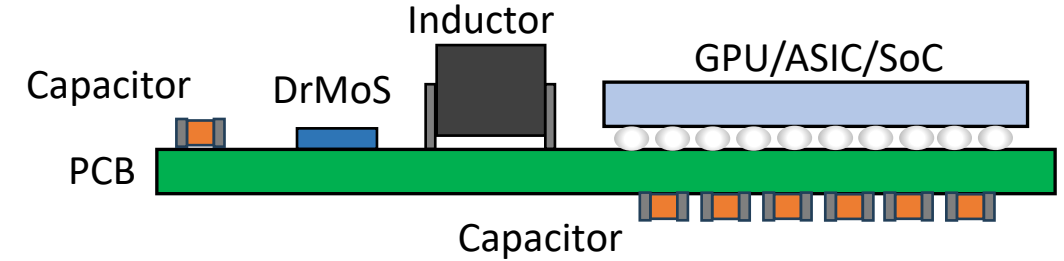
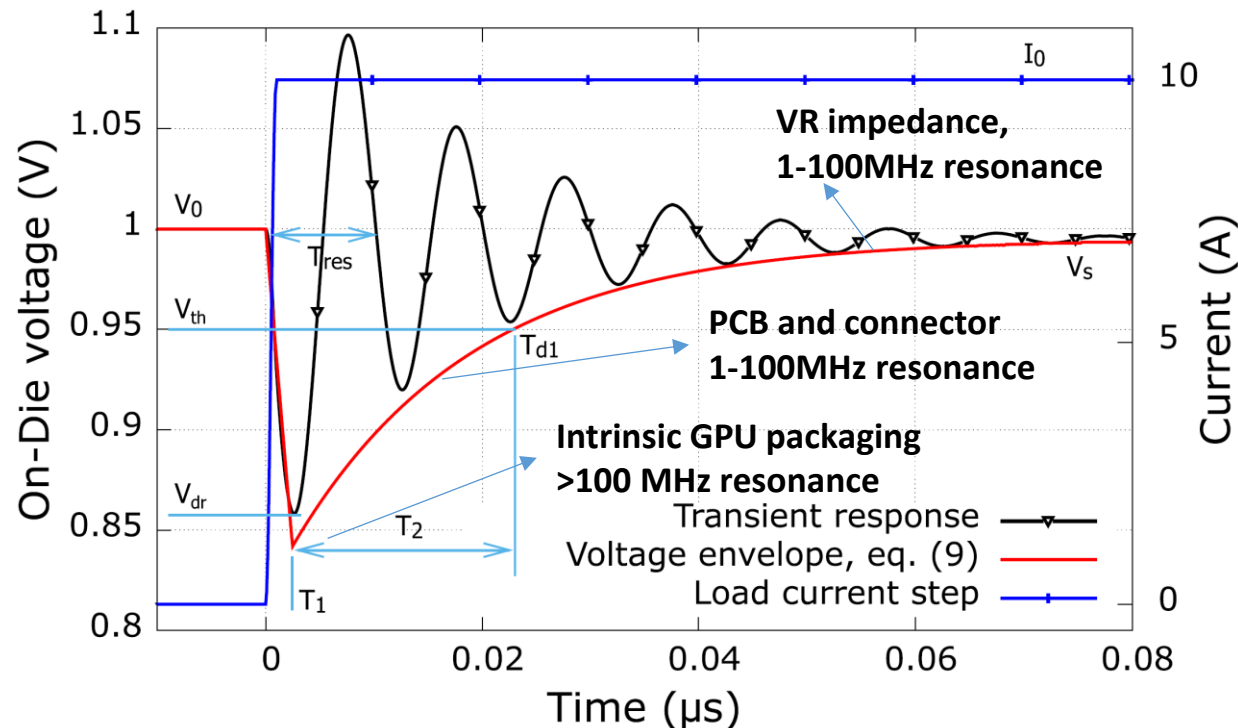
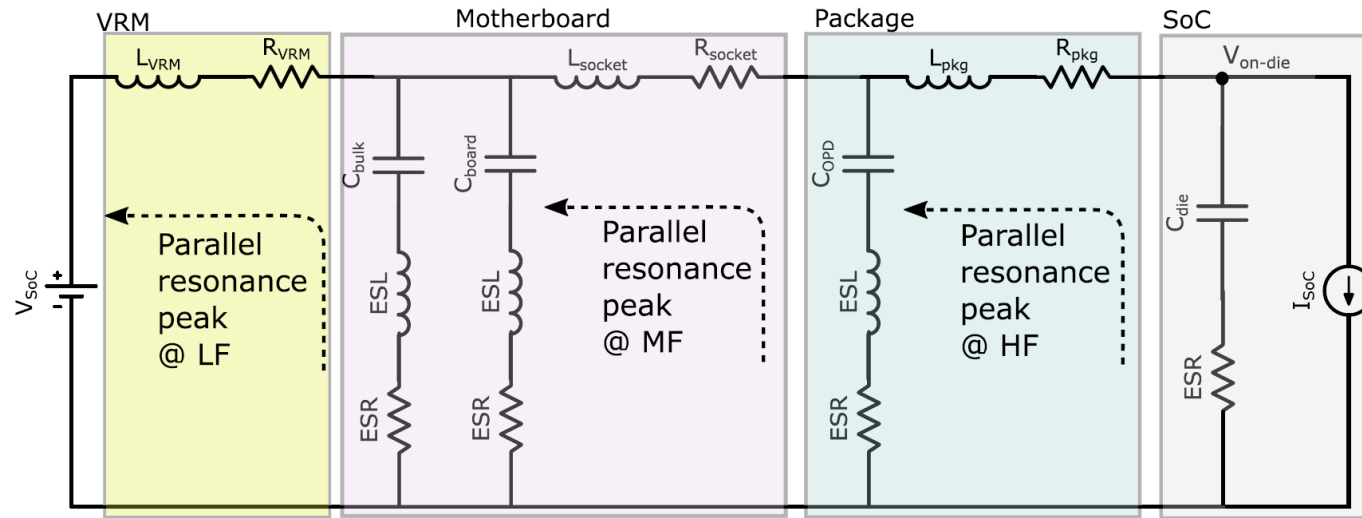
4-Phase integrated VR Module:

- **Customized DrMOS** with improved output pins to optimize PCB layout.
- **Embedded inductor**—reduces copper losses and side plates.
- **Embedded output capacitor**—uses special 0402 capacitors, with 800uF embedded output capacitance per module.

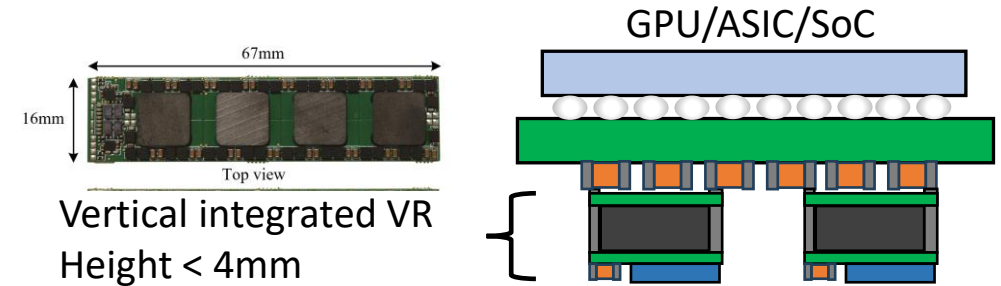
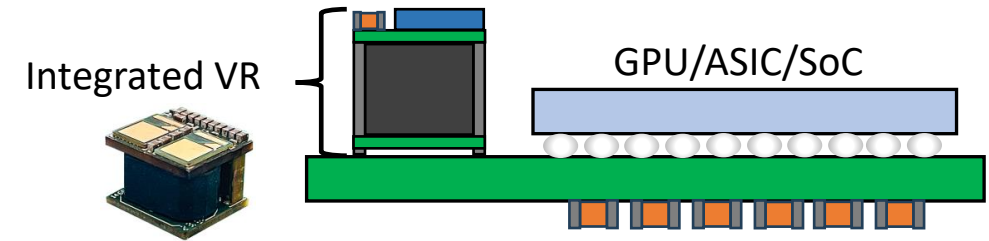
Top: inductor → better coupling

Middle: DrMOS → issue in cooling

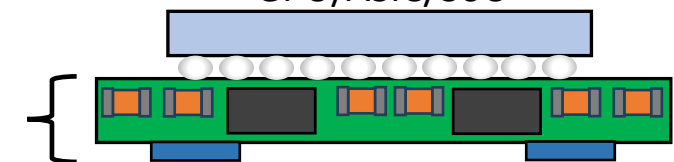
Location, Location, Location → miniaturised power supplies



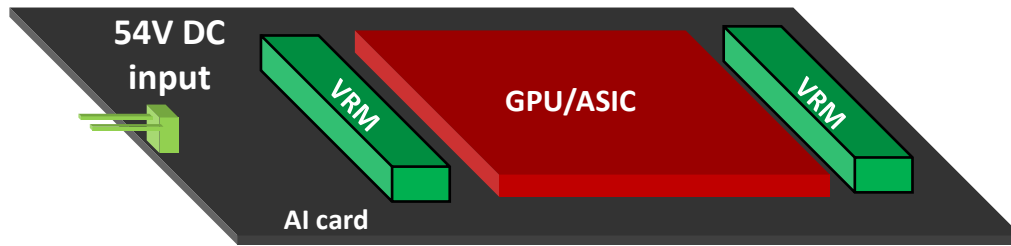
➤ Reducing distance from VR to GPU → reducing PDN loss and increase dynamics response



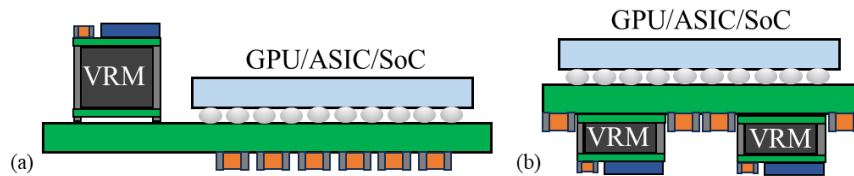
Vertical VR with PCB embedded L&C



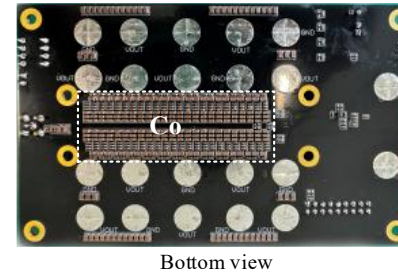
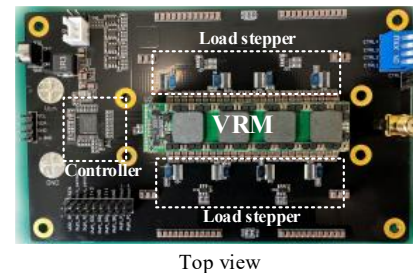
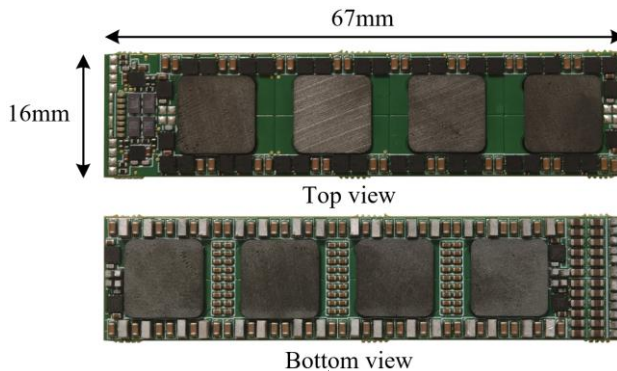
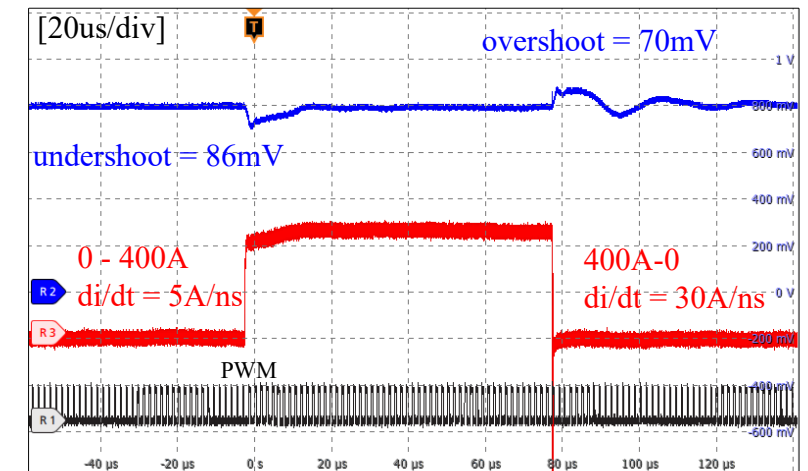
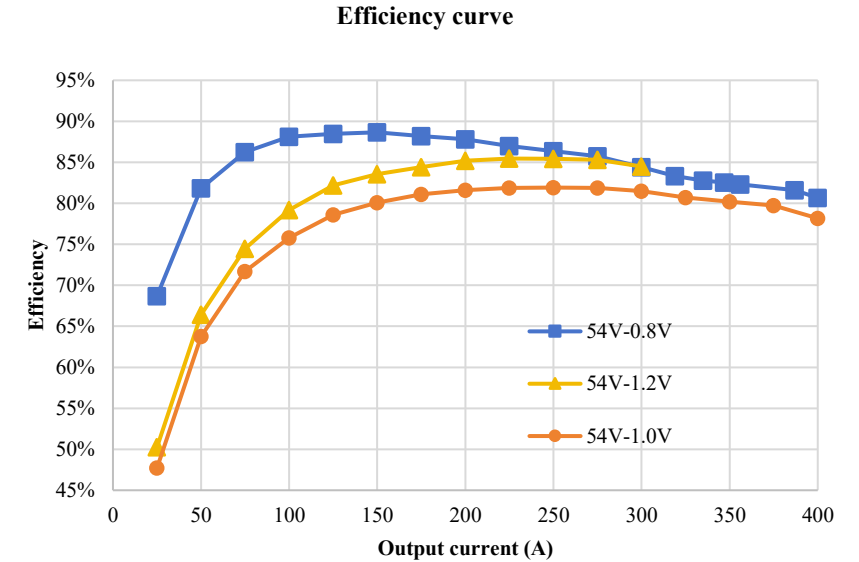
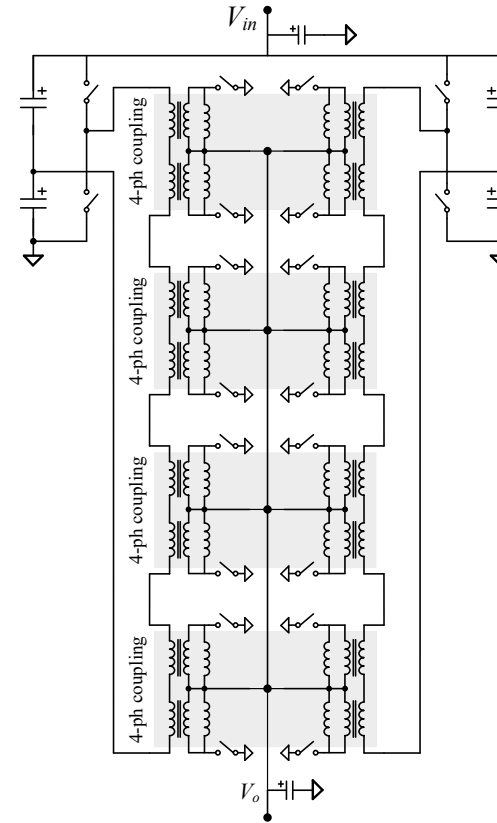
Advanced Single-Stage Regulate VR module (54-0.8V)



- ❑ Direct 54V to PoL regulated GPU voltage (<1V)
- ❑ High current module (>400A)
- ❑ High dynamic (low transient inductance)
- ❑ Miniaturised, smaller than GPU chip

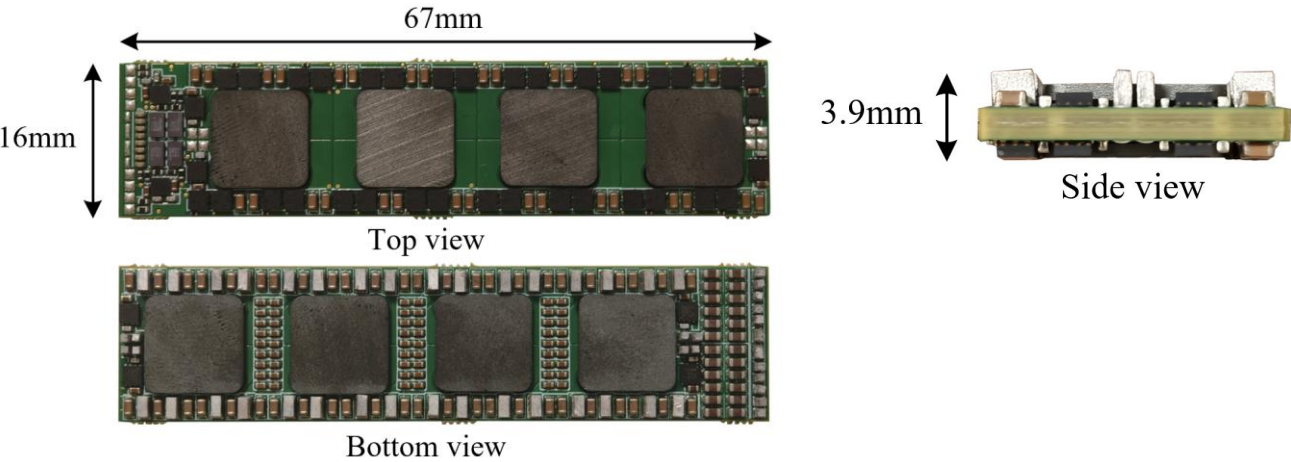


- ❑ Vertical and lateral mounting
- ❑ Integrated MLCC array (GPU core specific)



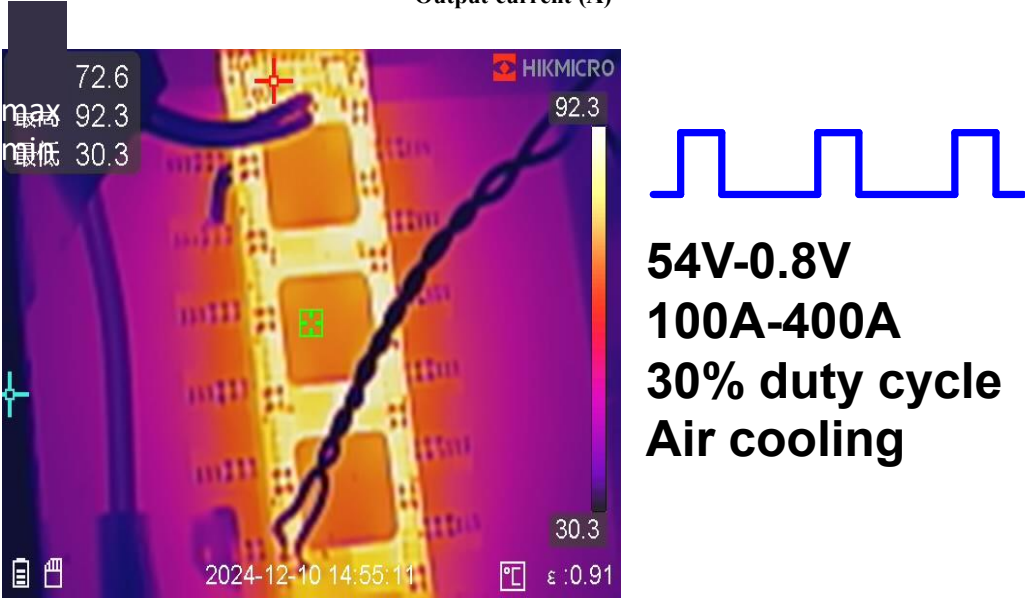
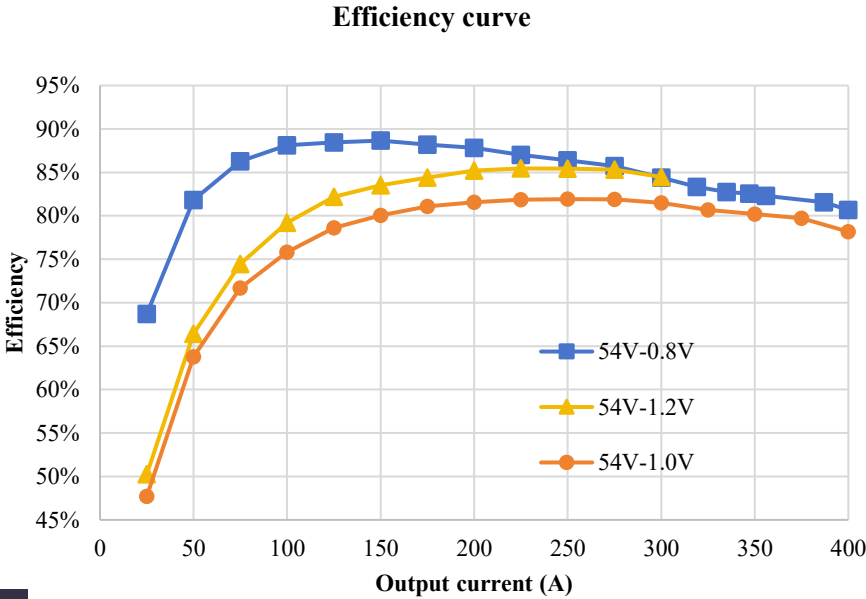
- ❑ **Cambridge prototype**, integrated magnetics, 450A, 54-0.8V, 67 x 16 x 3.9mm
- ❑ Dynamic response test di/dt 5A/ns, <80mV voltage transient
- ❑ End-to-end peak efficiency 90% @30% load

Prototype



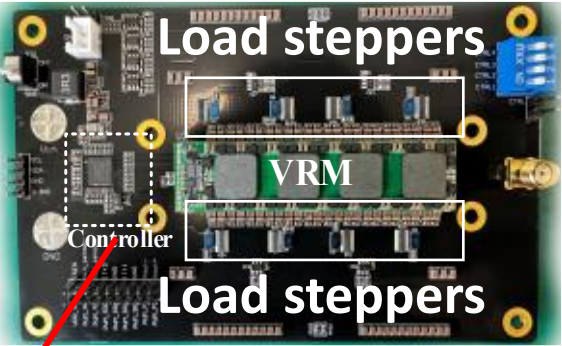
Input voltage	40V-60V (typically 54V)
Output voltage	0.8V-1.2V (typically 0.8V)
Output current	400A
Switching frequency	600kHz
Module dimension	67mm/16mm/3.9mm (L/W/H)
Lss per phase	68nH
Ltr per phase	13nH

- Ultra-low profile (3.9mm thickness) design for VPD
- Output current 400A in 67 x 16 x 3.9mm
- End-to-end peak efficiency 89%, full-load efficiency 81%

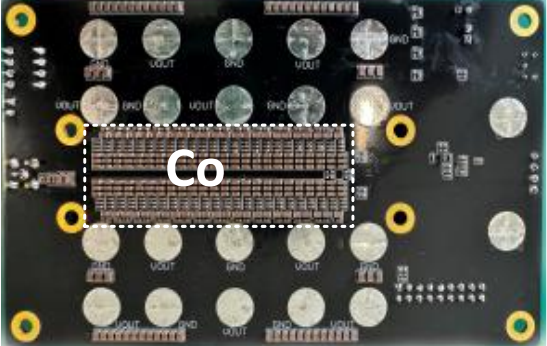


Dynamic testing

Dynamic EVB with load steppers

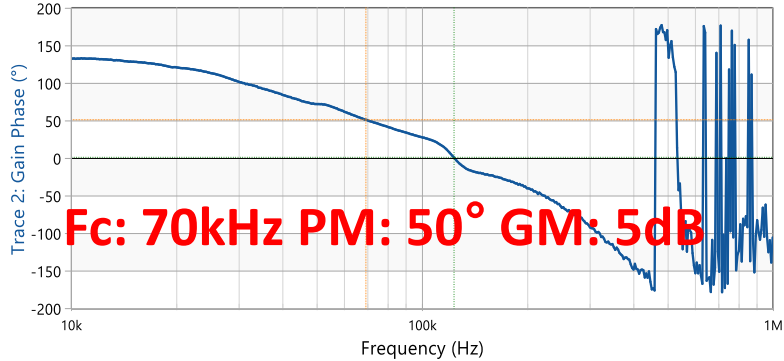
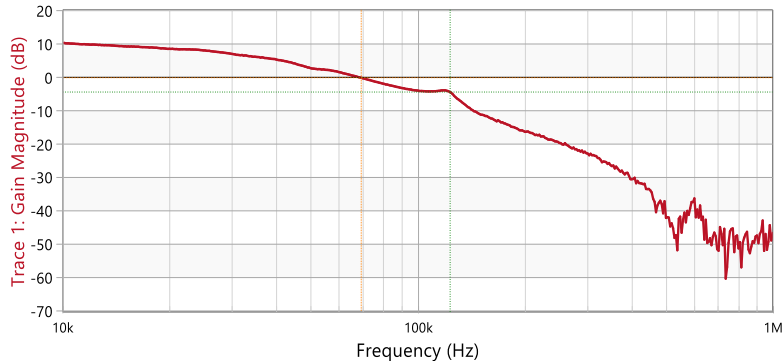


Top view

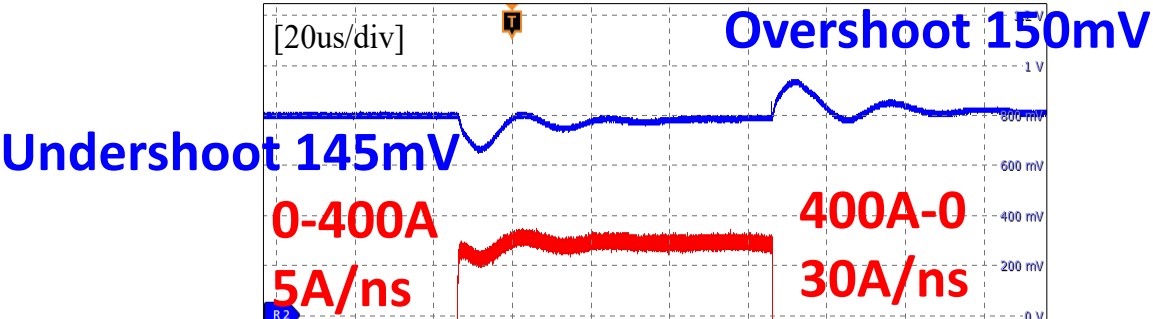
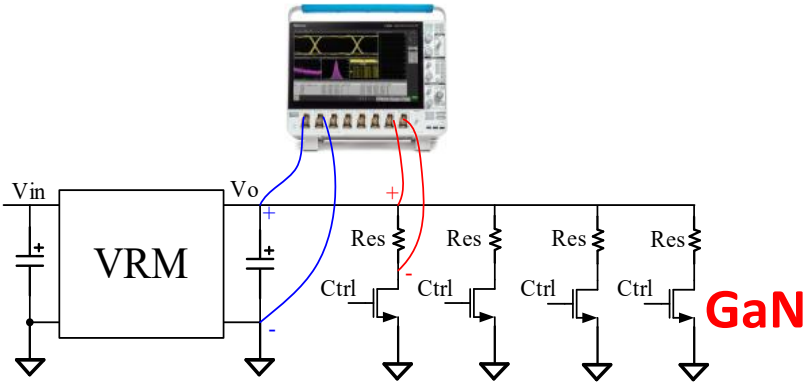


Bottom view

IFX XDPP-1100

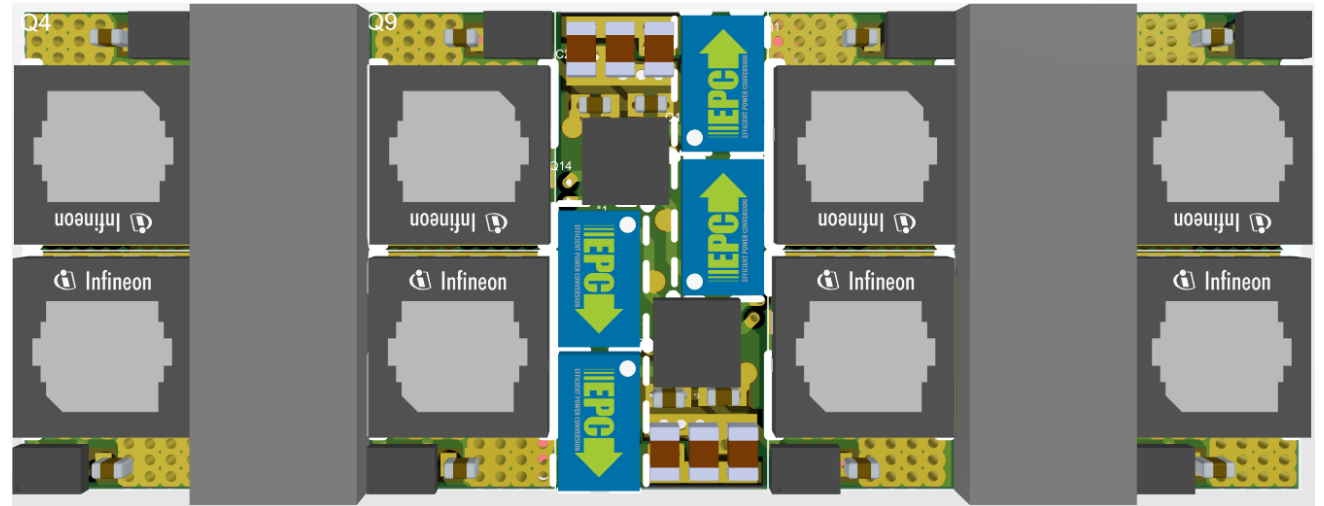
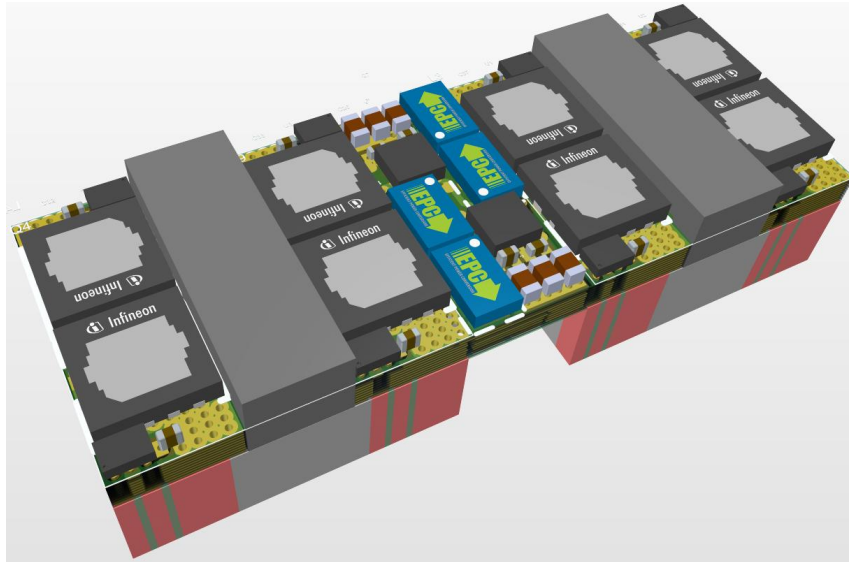


Fc: 70kHz PM: 50° GM: 5dB



- GaN based dynamic evaluation board
- Ultra-fast transient response ($L_{tr} = 13nH$, PID control)

Single-Stage Vertical Voltage Regulator



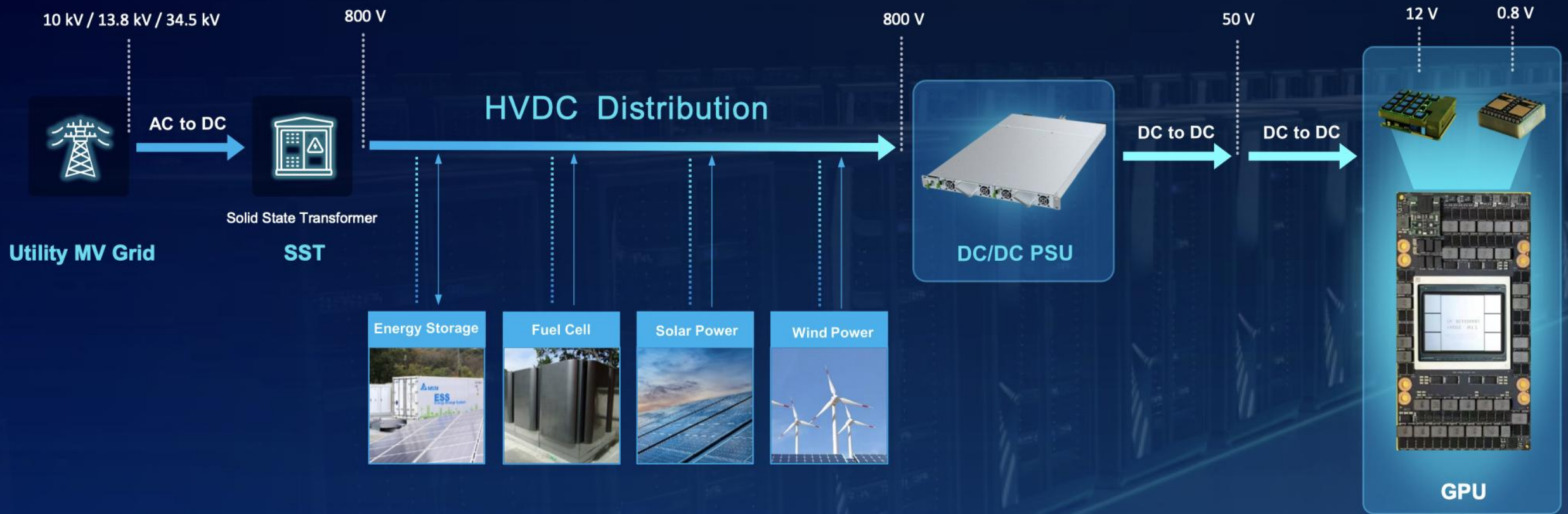
Prototype- 24mm(length) x 9mm (width) x 5.6mm (height)

Current density: $1.48\text{A}/\text{mm}^2$

Inductor: 3mm, PCB: 1.2mm, transformer: 1mm, bottom board: 0.4mm(not shown)

Future power architecture for AI datacentre

Long Term Data Center Infrastructure: From MW to GW



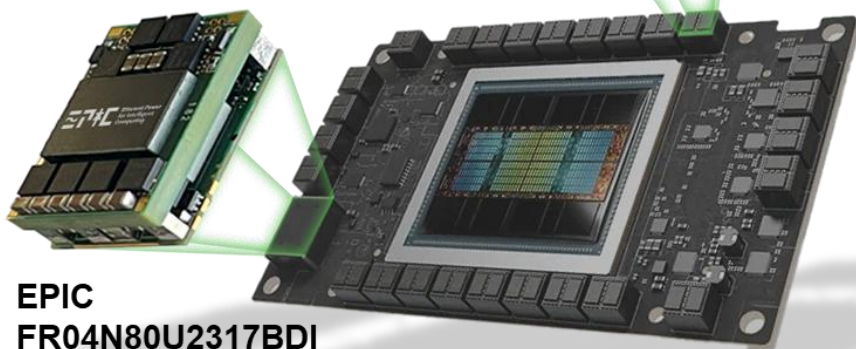
Courtesy to **Delta Electronics**

EPIC Tech Ltd

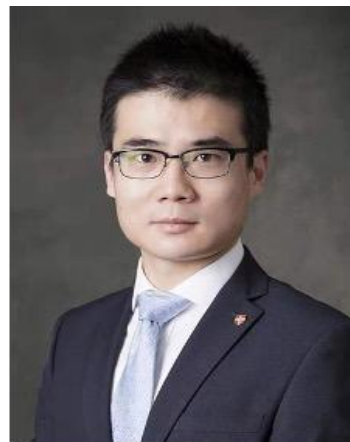
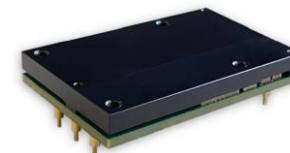
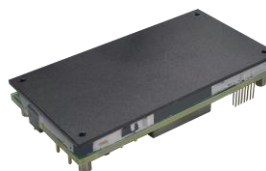


Efficient Power
for Intelligent
Computing

EPIC
VR12N80U1009BAA



EPIC
FR04N80U2317BDI



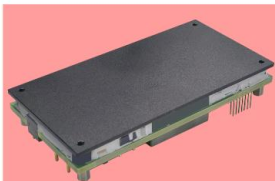
Prof Teng Long
Founder, Chairman

- Tenured Full Professor at the University of Cambridge, world-renowned scholar in power electronics
- Founder and Director of the Cambridge University Advanced Power Electronics Laboratory
- Deputy Director of the Cambridge University Nanjing Centre for Technology Innovation
- Published over 100 SCI journal papers, secured more than £5 million in research funding, holds 15 Chinese patents and 7 international patents
- Formerly with General Electric (GE) UK Power Conversion Division, Chartered Engineer (UK)

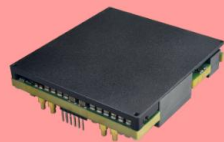


Michael Xu
Co-founder,
CEO

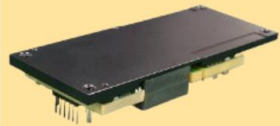
- Bachelor's and Master's degrees in Power Electronics from Zhejiang University; General Manager Program at China Europe International Business School (CEIBS)
- 2009–2018: Co-founder and R&D Director of Inventronics, major contributor to its A-share IPO
- 2018–2024: Second employee of Navitas China, Head of Application R&D, major contributor to Navitas's NASDAQ IPO
- Zhejiang Province's "151" Talent Program and Hangzhou's "131" Mid-level Talent Program; holder of 18 invention and utility model patents



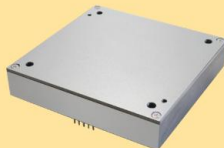
800-48V Regulated
In: 620-950V, Out: 48V
Full-Brick
2.8-3.5 kW, 97.2% peak



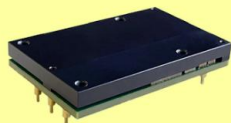
800-50V Fixed-Ratio
In: 650-900V, 16:1,
Half-Brick, Full-Brick
6-10 kW, >98% peak



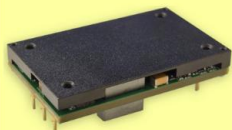
400-50/25V Fixed-Ratio
In: 250-460V, 16:1, 8:1
1/4-Brick, Isolated
1.8-2kW, 98% peak



300-30V Regulated
In: 220-330V, Out: 30V
Half-Brick, Isolated
1-1.5kW, 95.8% peak



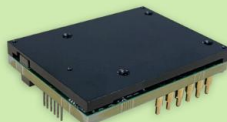
48-12V Regulated
In: 40-60V, Out: 12V
1/4-Brick, Non-Isolated
1.8-2kW, 98.7% peak



48-12V Regulated
In: 48-60V, Out: 12V
1/4-Brick, Isolated
800W, 97.6% peak



30-12V Regulated
In: 16-40V, Out: 12V
1/8-Brick, Isolated
300-400W, 95.2% peak



48-3.3V Regulated
In: 25-60V, Out: 3.3V
Half-Brick, Non-isolated
400A@3.3V, 96.5% peak



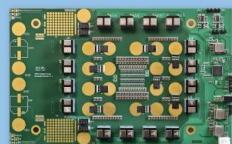
48-6V Fixed-Ratio
In: 40-60V, 8:1
23x17mm, Non-Isolated
0.5-1kW, >97% peak



48-12V Fixed-Ratio
In: 40-60V, 4:1
23x17mm, Non-Isolated
1-1.5kW, 98.3% peak



12-1V Regulated
In: 4.6-16V, Out: 0.23-5V
9x8x10/4.8mm
140A@0.8V, >96% peak



16-Phase 12-1V parallel
In: 48/12V, Out: 0.5-2V
1000A continuous
Up to 4000A/ μ s transient



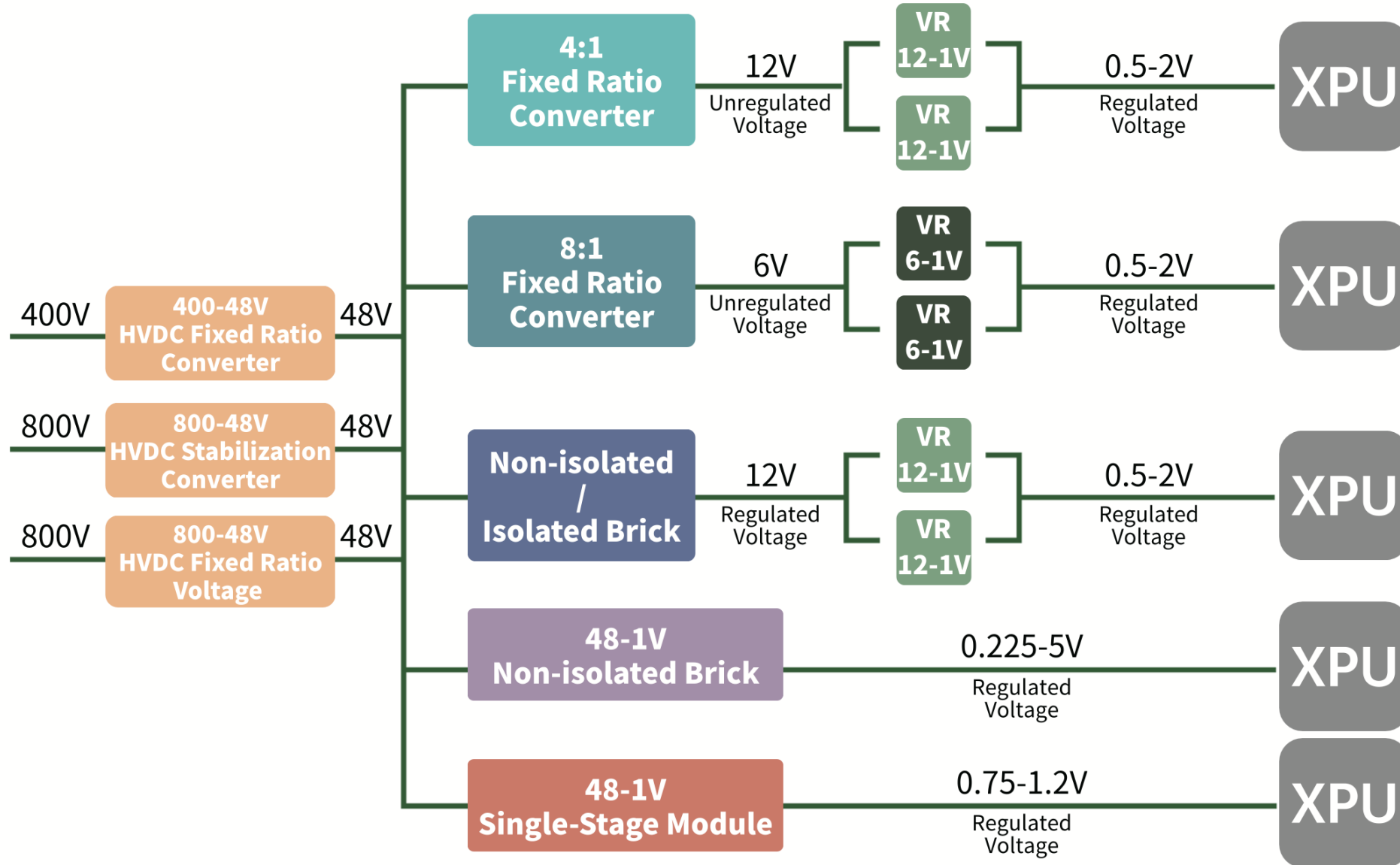
48-1V Fixed-ratio
In: 40-60V, 48:1
58x115x5.6mm, Non-Iso
450A@0.8V, >93% peak



54-1V Regulated
In: 40-60V, Out: 0.75-1.2V
67x16x3.9mm, Non-Iso
450A@0.8V, >90% peak



Datacenter Power Delivery Architectures



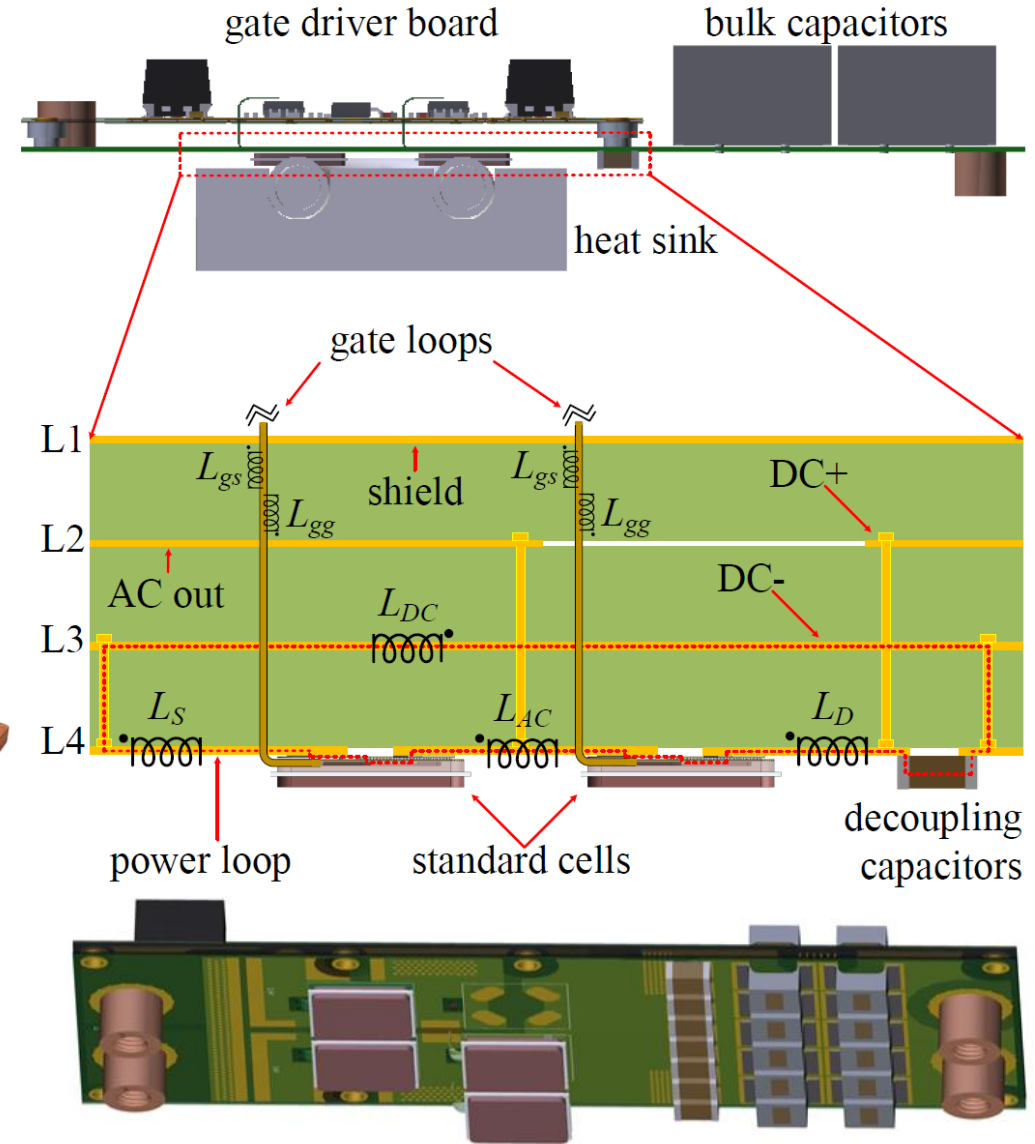
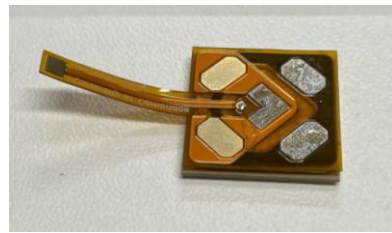
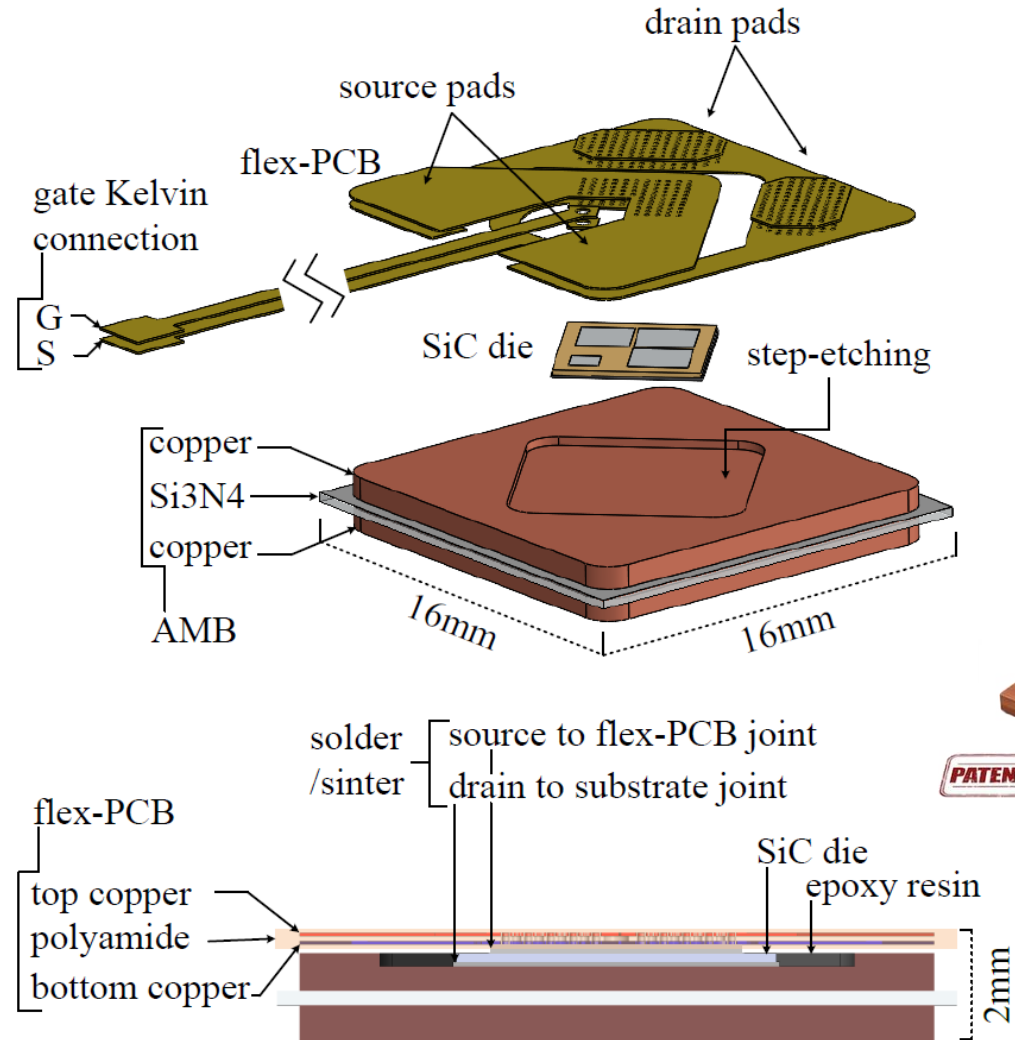


www.epicpowers.com
info@epicpowers.com

Contents

- State-of-the-art Power Supply Architecture for AI datacentres
- **Advanced Power Electronics Packaging for for High Integration**
- Smart Soft-Switching using Electroluminescence

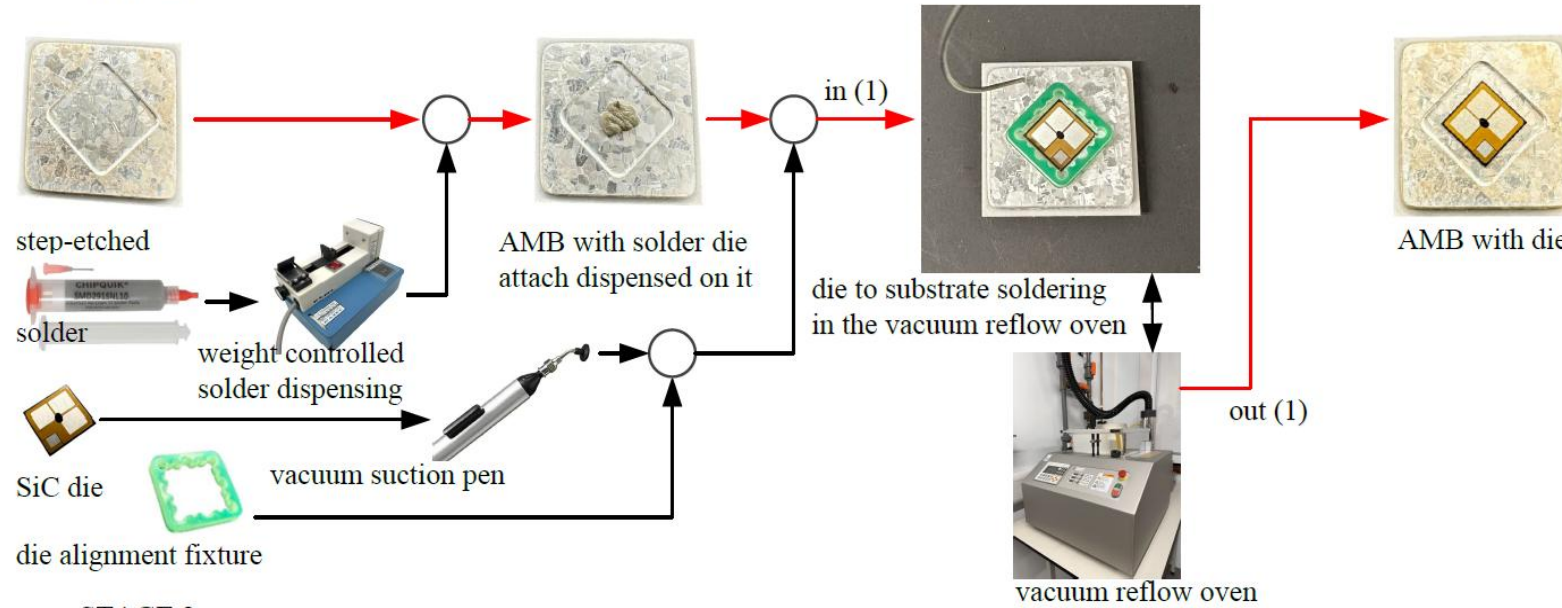
Standard Cell concept and structure



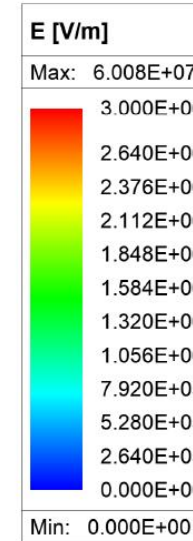
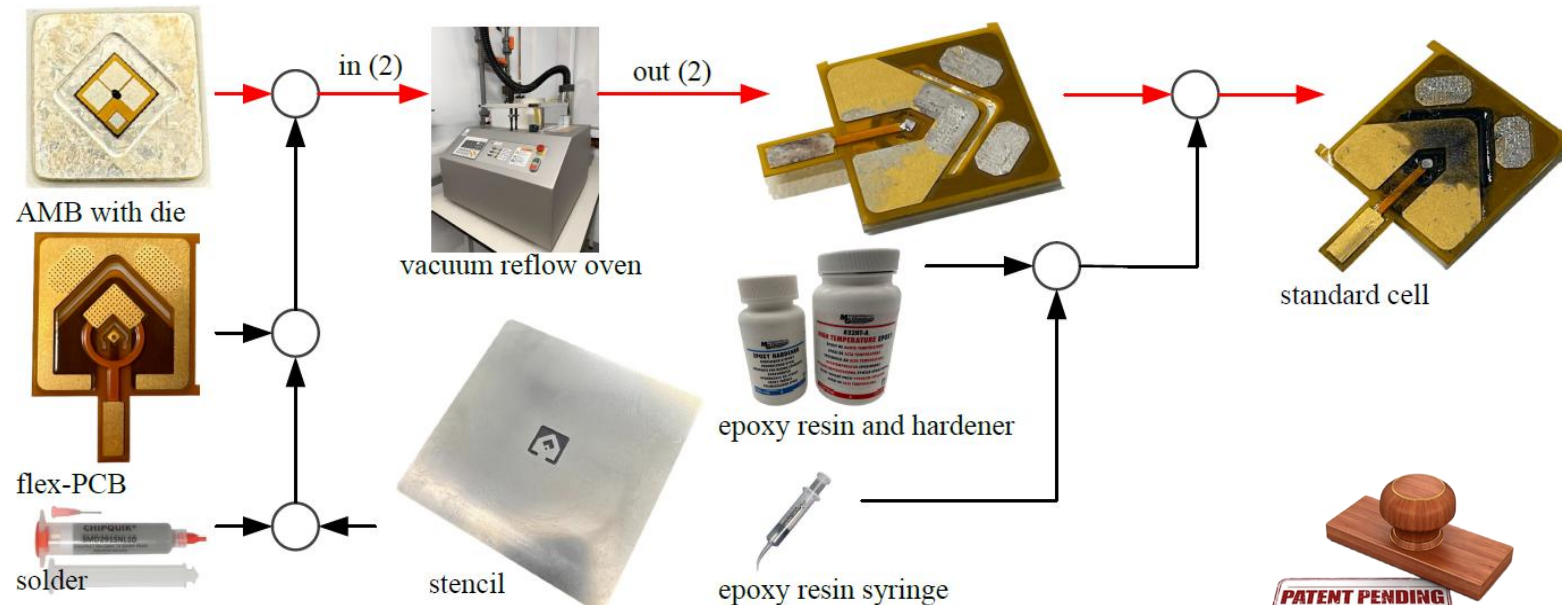
A. Janabi *et al.*, "Substrate Embedded Power Electronics Packaging for Silicon Carbide mosfets," in *IEEE Transactions on Power Electronics*, vol. 39, no. 8, pp. 9614-9628, Aug. 2024

Standard Cell device package assembling

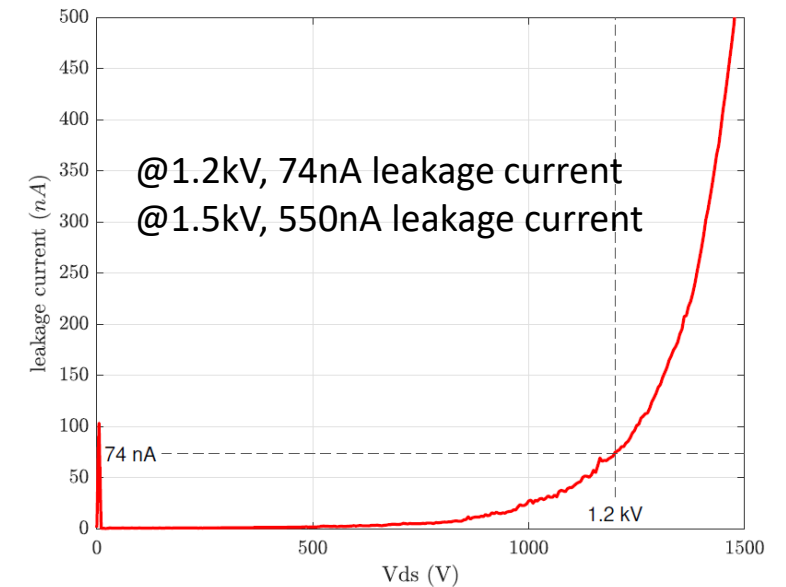
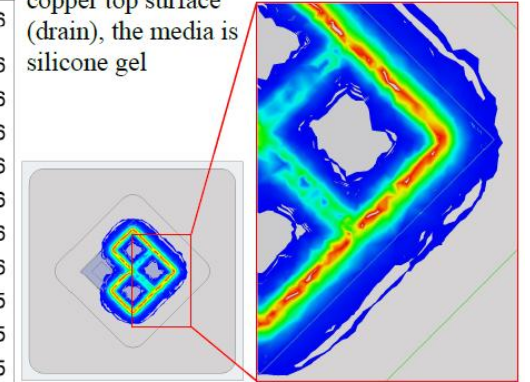
STAGE 1



STAGE 2

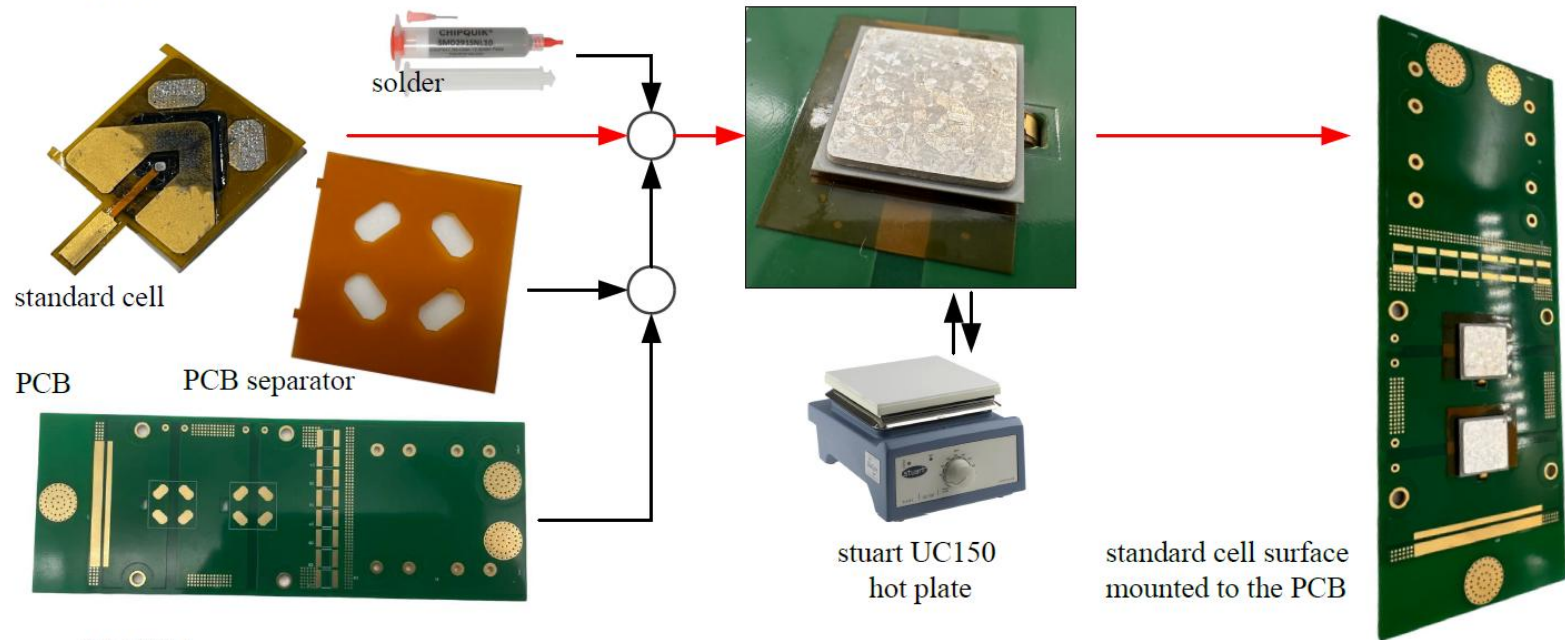


E-field between the source pads and the copper top surface (drain), the media is silicone gel

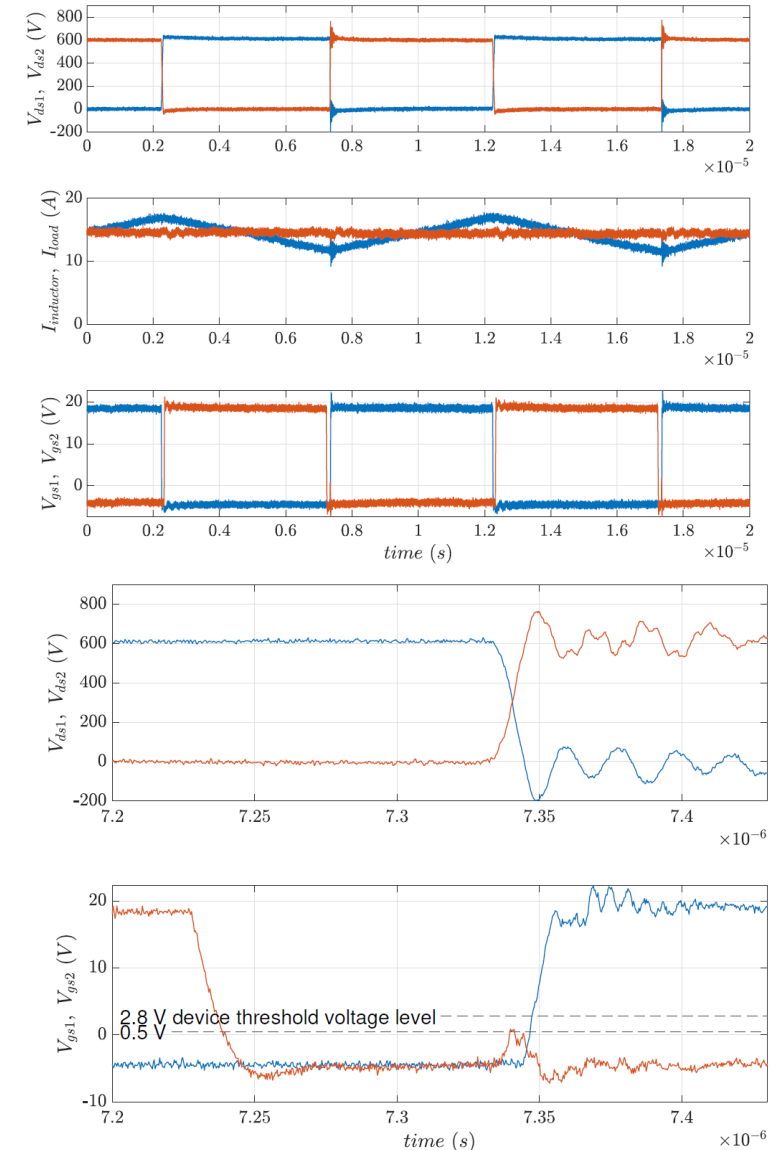
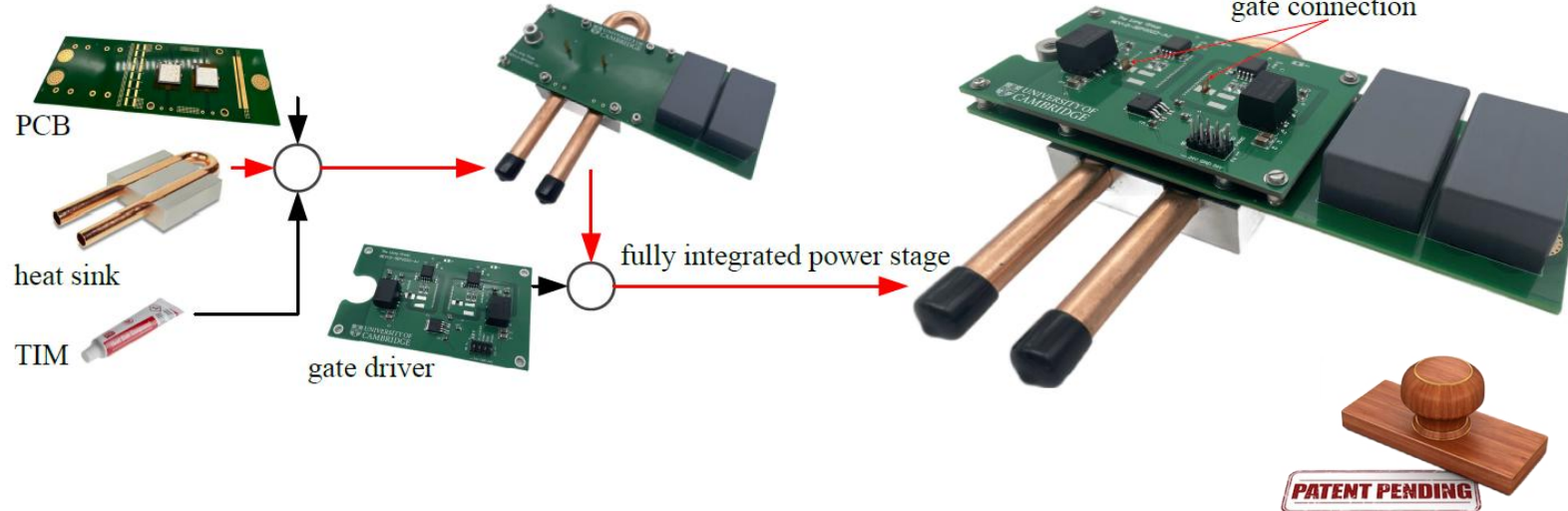


Standard cells in converter systems – surface mounted

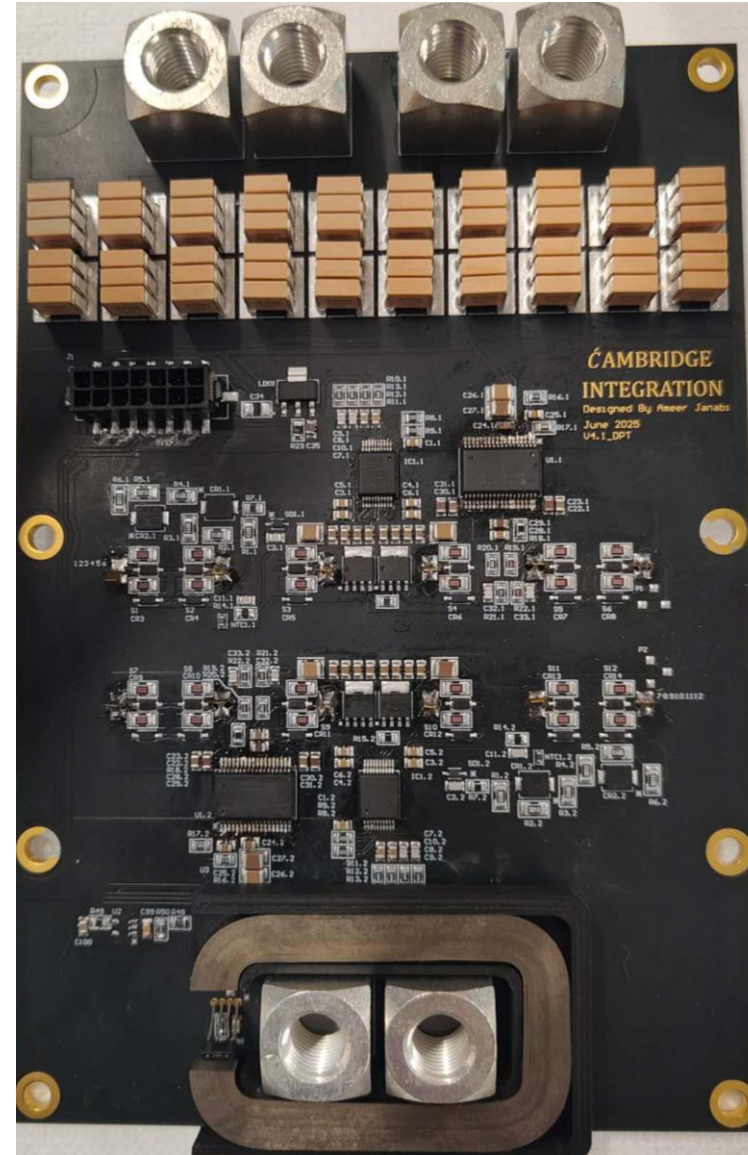
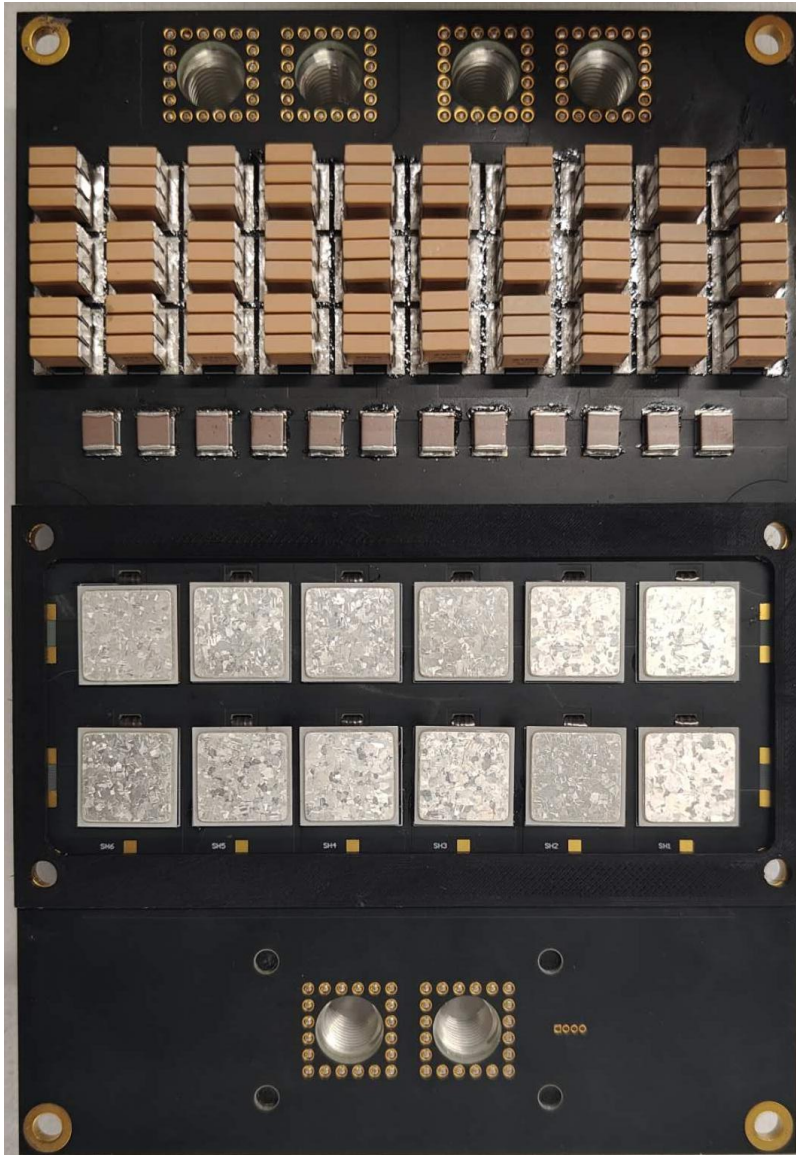
STAGE 3



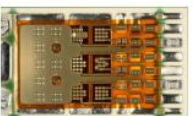
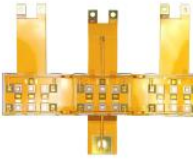
STAGE 4

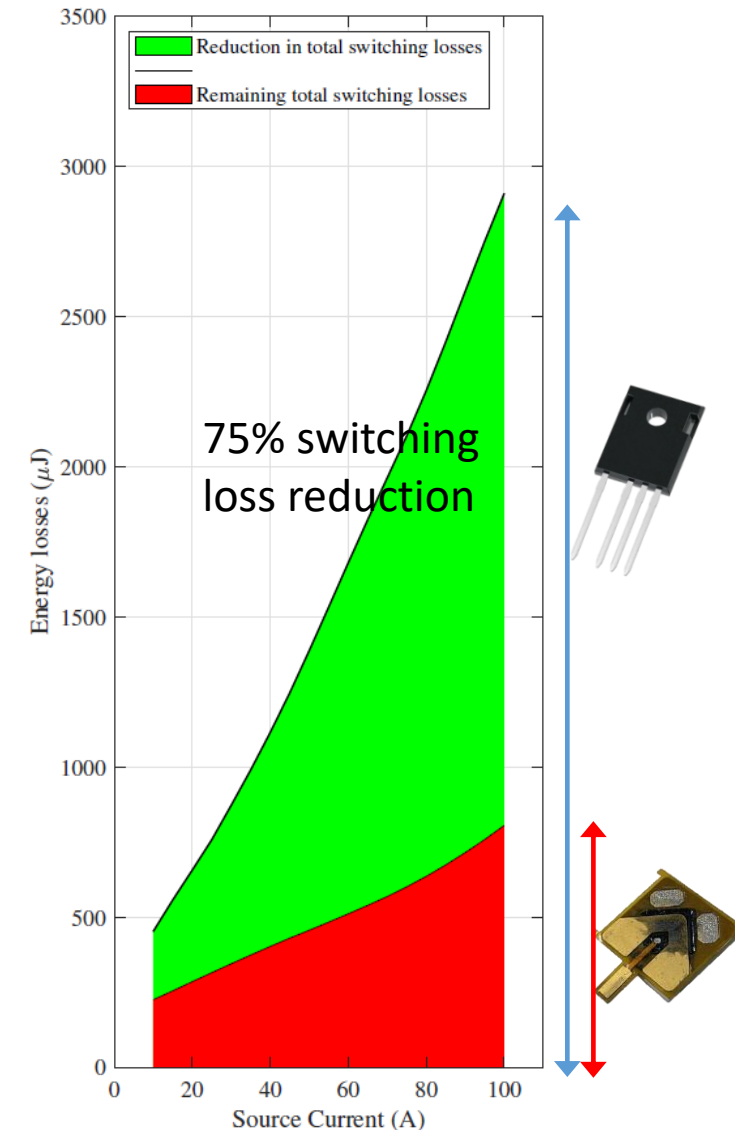
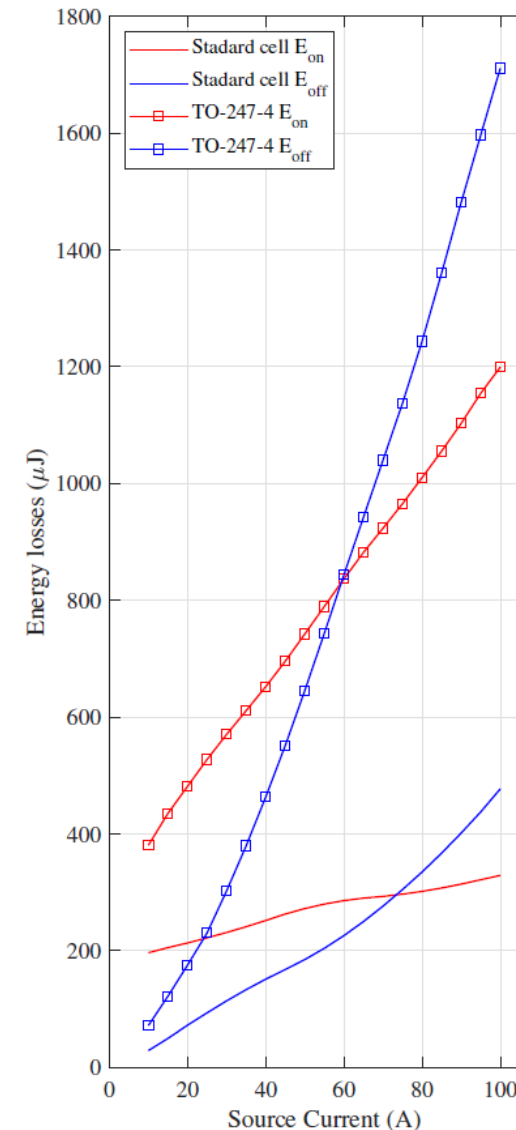


320 kW/L power assembly using 6 Standard Cells in parallel



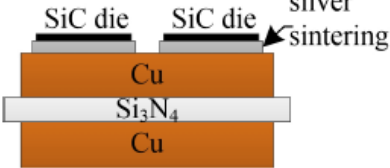
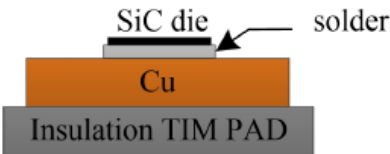
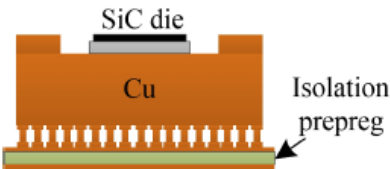
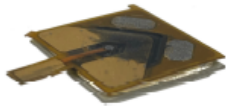
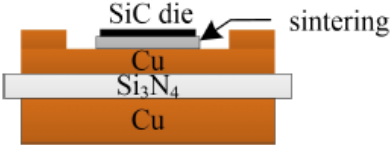
Very low switching energy of standard cell due to low inductance

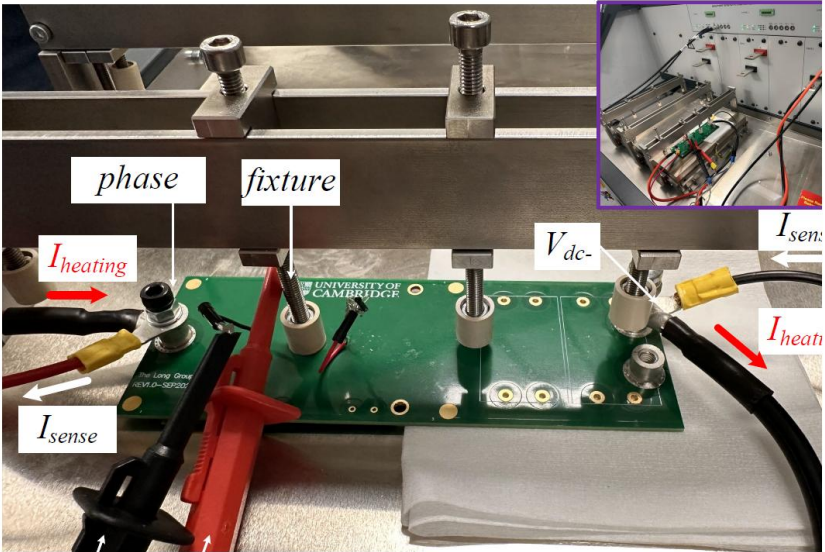
Package type	Illustration	$L_g(nH)$	$L_p(nH)$
ST P AK/IDPAK		20*	21*
TO-247-4L/TO247plus		20.5*	36.9*
Schweizer p^2 Pack		Low/ layout depend- ent	1.45 ^[22]
AG (AT&S)/CPES		2.2 ^[16]	2.3 ^[16]
GE POL-kW		(20 – 30)*	2.6 ^[36] , 5 ^[37]
Semikron eMPack®/SKiN		(20 – 30)*	(2.5 – 6)**
3D-Hybrid package		(20 – 30)*	2.4 ^[35]
Proposed standard cell		1.5*	0.716*, 1**



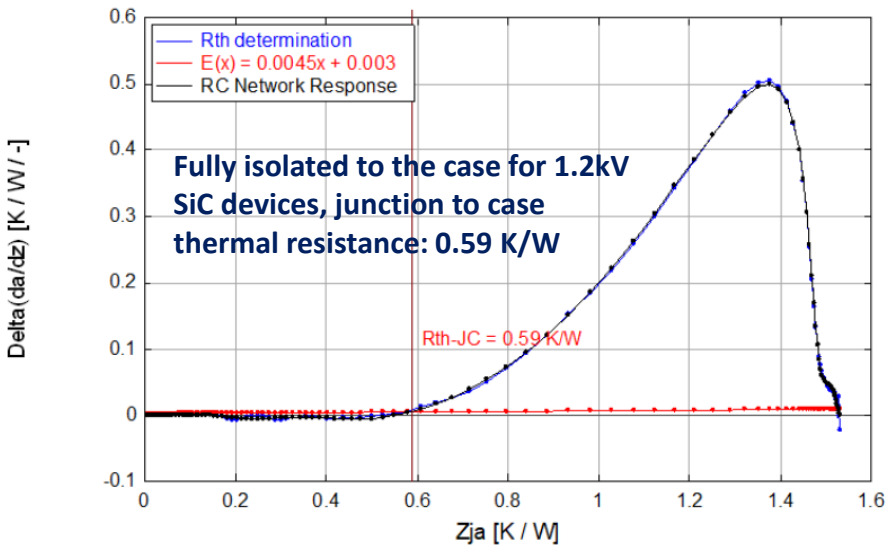
STMicroelectronics SiC die chip:
SCT116N120G3DXAG, 1.2kV, 14. 6mOhm, 130A

Low thermal resistance of standard cell

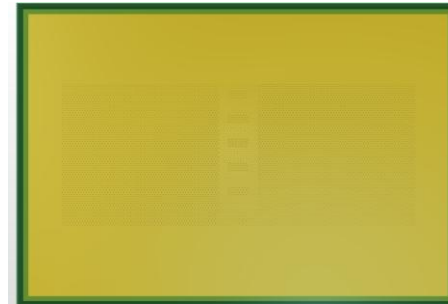
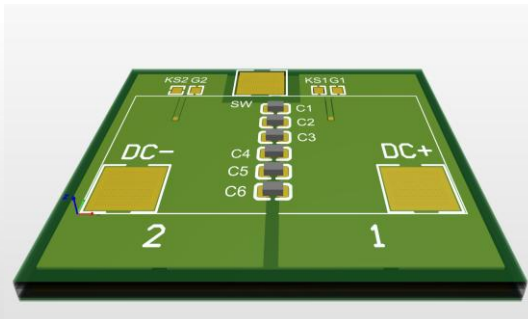
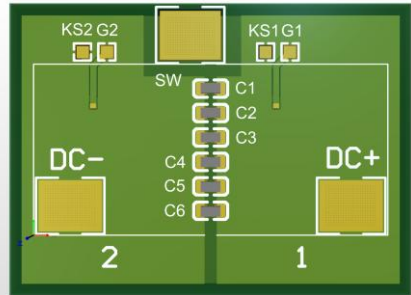
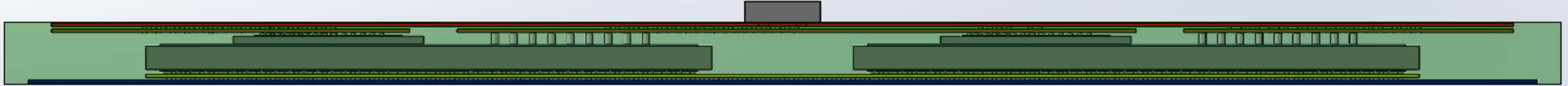
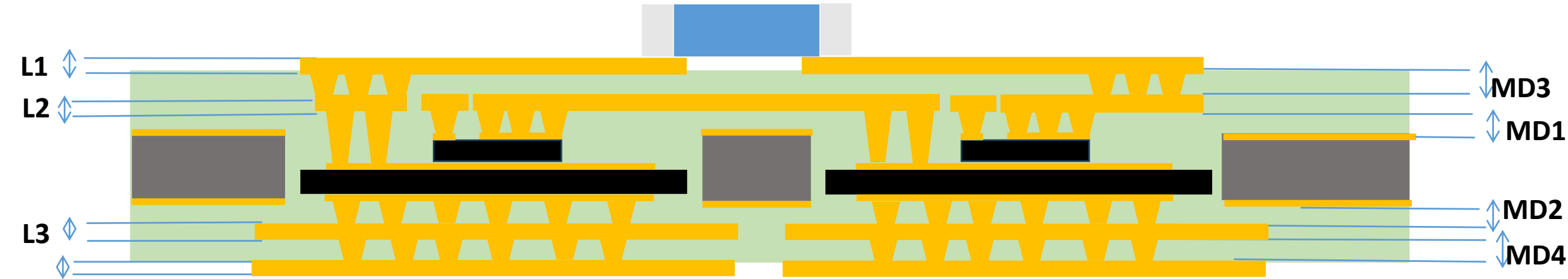
Package type	Illustration	Layers stack	R_{th-JC}
ST PAK/IDPAK			0.6 ^[45]
TO-247-4L/TO247plus			1.3
Embedding/ p^2 Pack, ABB			Only for 48V system! 0.58, 0.5 ^[47]
Proposed standard cell			0.59



T3Ster Master: Difference of the derivatives

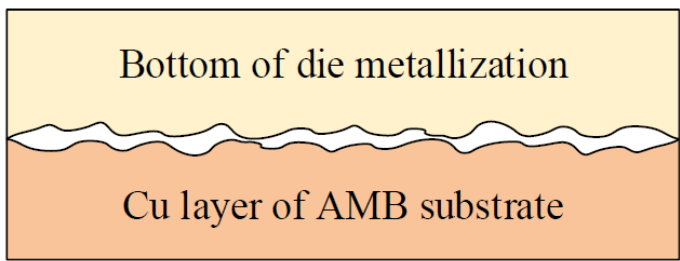
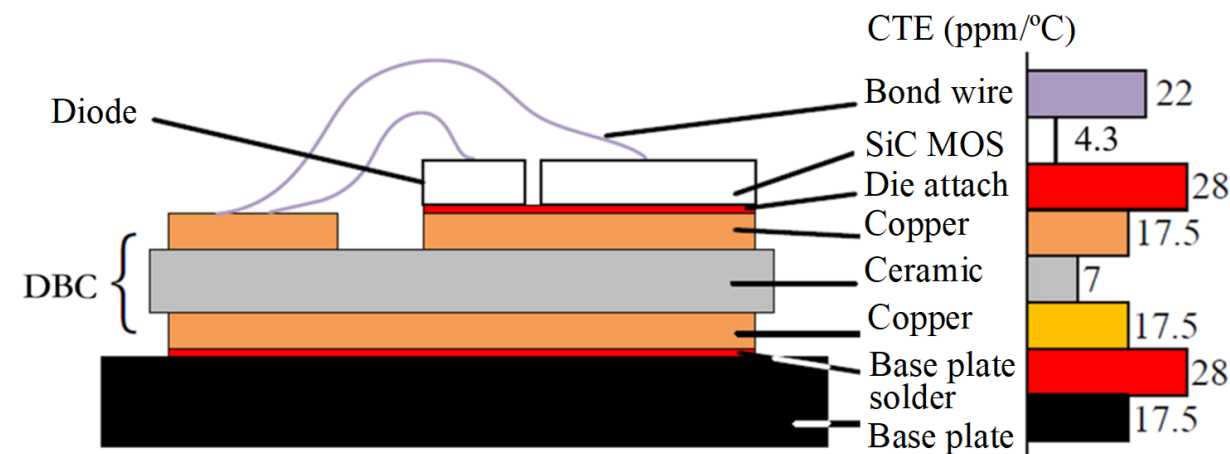


Beyond Standarc Cell: PCB embedded SiC/diamond substrates

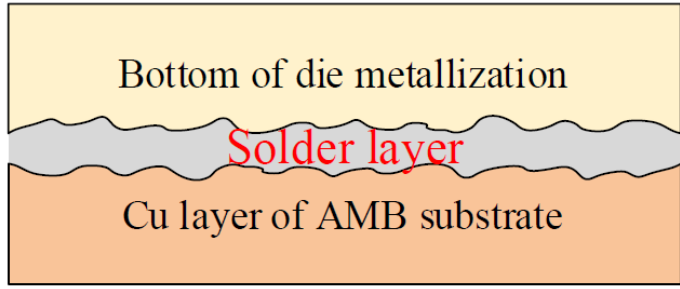


- Insulation for 1.2kV applications
- Much higher thermal conductivity
- Less than 300pH half-bridge stray inductance

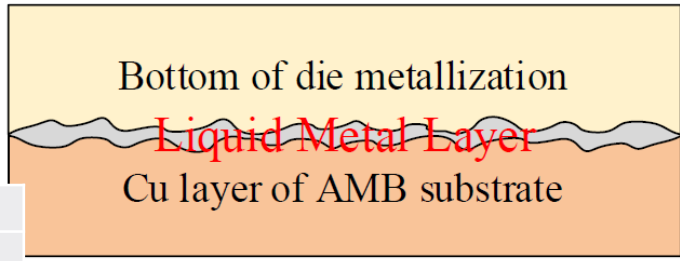
Basics of thermomechanical stress of power electronics package



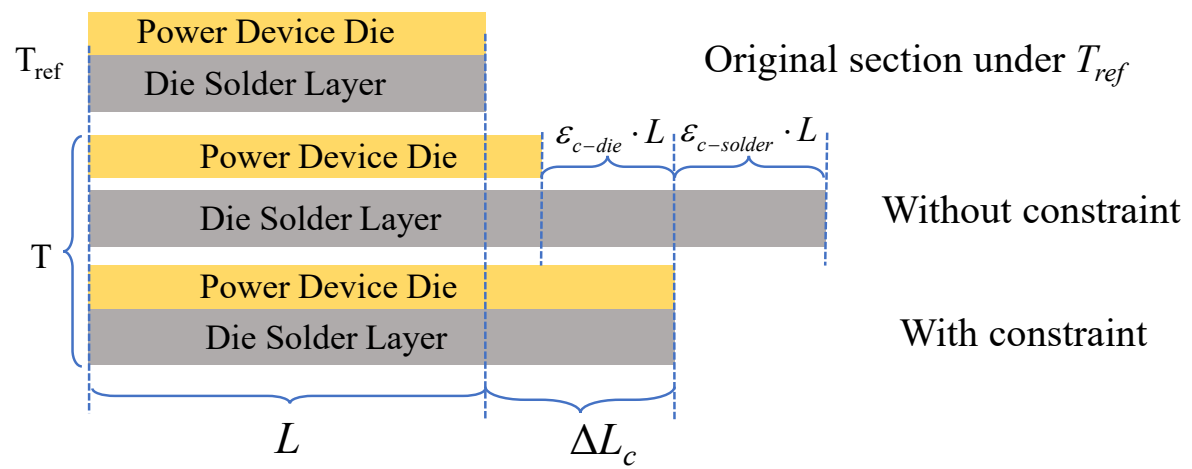
(a)



(b)

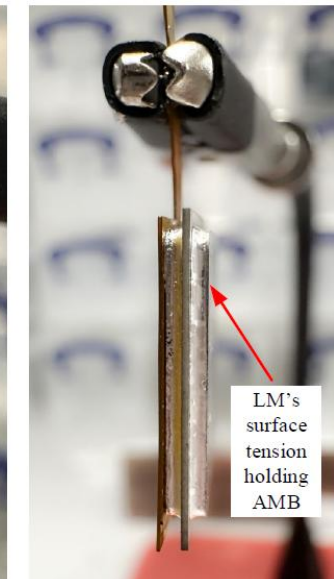
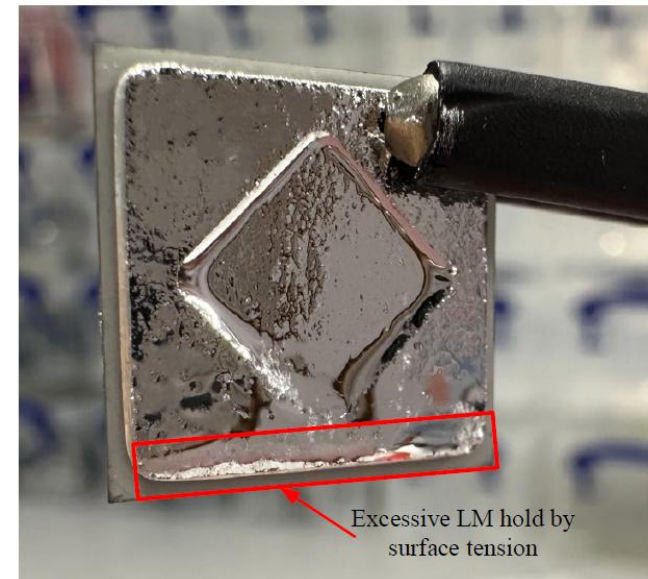
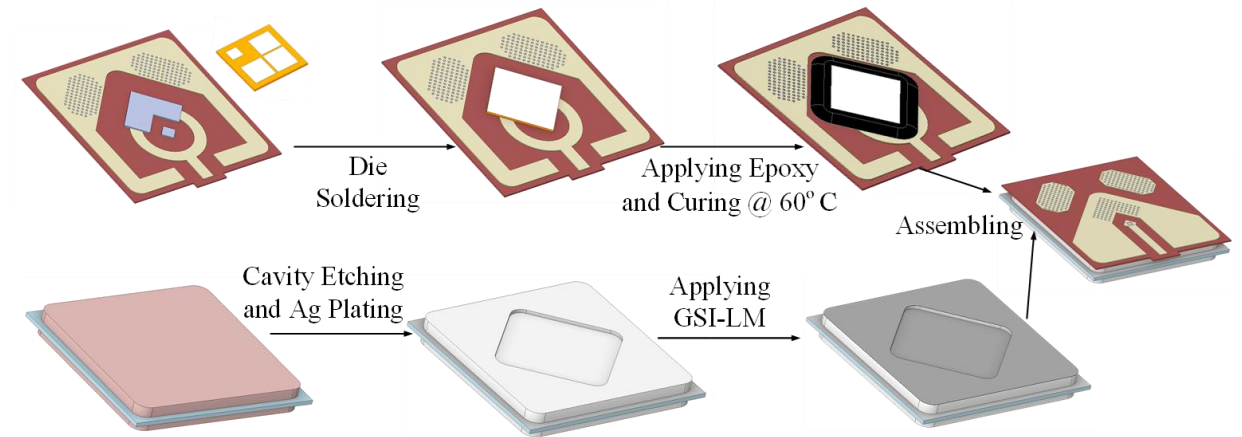
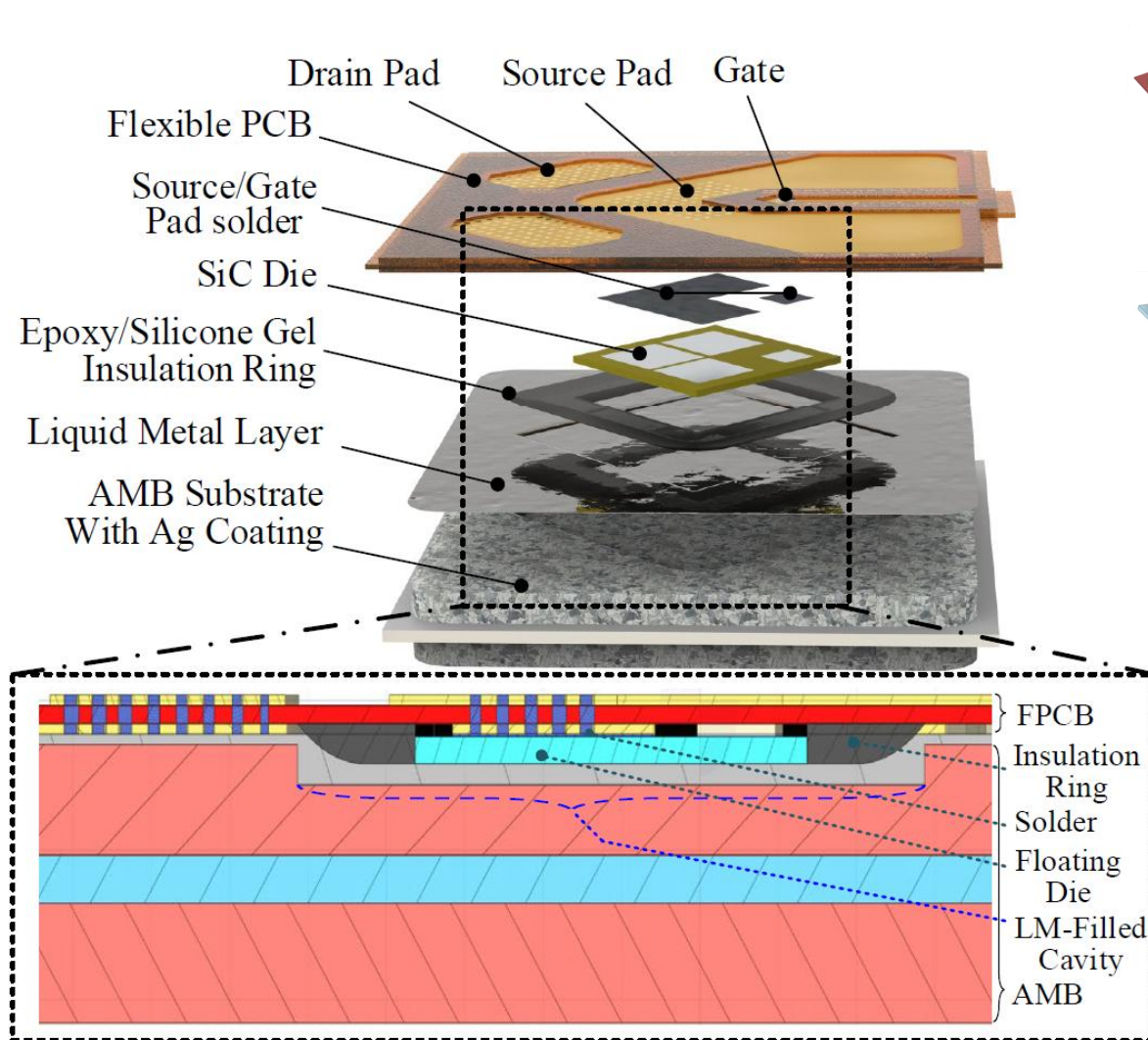


(c)



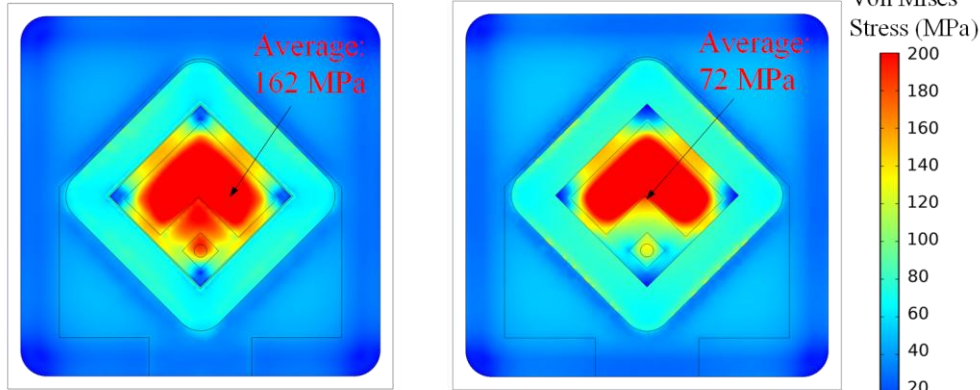
Material	Key material properties		
	(°C)	(S/m)	(W/(m•K))
GaInAg	8	5.0×10^6	75
Ga ₆₈ In ₂₂ Sn ₁₀	-17	3.46×10^6	16.5
In ₅₁ Bi _{32.5} Sn _{16.5}	53	4.9×10^6	70
Solder (SAC305)	217	7.6×10^6	58.7

Using GalnAg LM for die touch joint



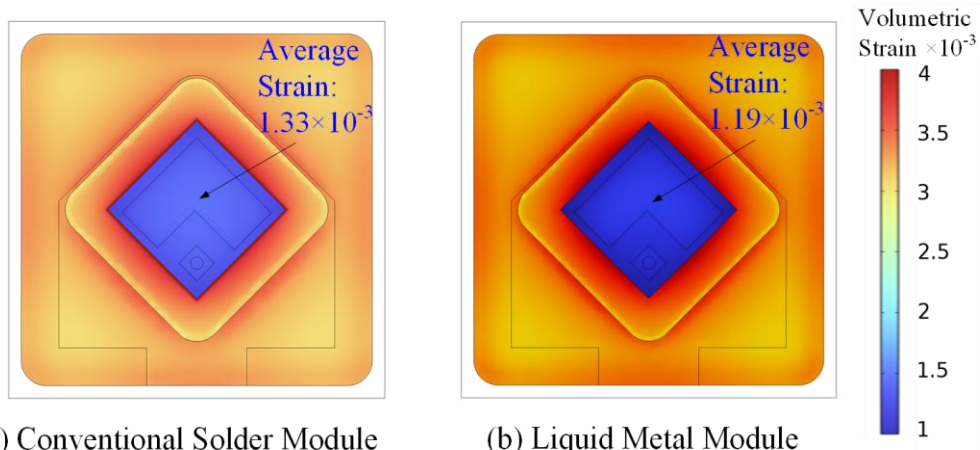
W. Mu, A. Janabi, B. Hu, L. Shillaber and T. Long, "Liquid Metal Fluidic Connection and Floating Die Structure for Ultralow Thermomechanical Stress of SiC Power Electronics Packaging," in *IEEE Transactions on Power Electronics*, vol. 39, no. 7, pp. 7808-7814, July 2024,

Large reduction of stress due to floating die structure using LM



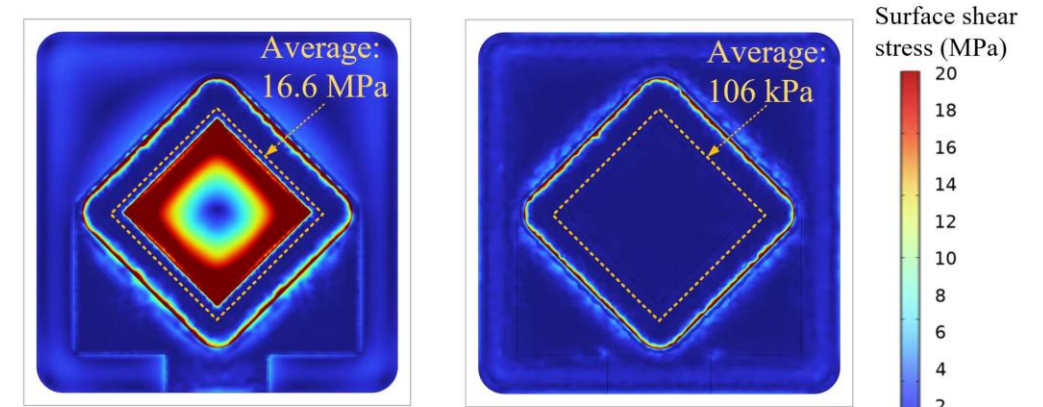
(a) Conventional Solder Module (b) Liquid Metal Module

- ❖ Von-Mises stress comparison
- 55% reduction on the SiC MOSFET



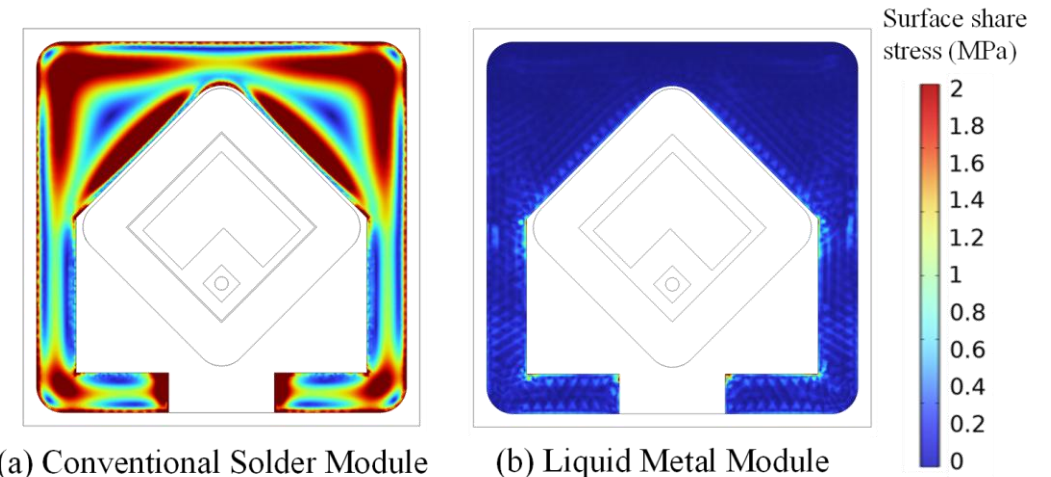
(a) Conventional Solder Module (b) Liquid Metal Module

- ❖ Volumetric thermal strain comparison
- Strain is decoupled by the LM layer so the die is under less tension.



(a) Solder-based Packaging (b) LM-based Packaging

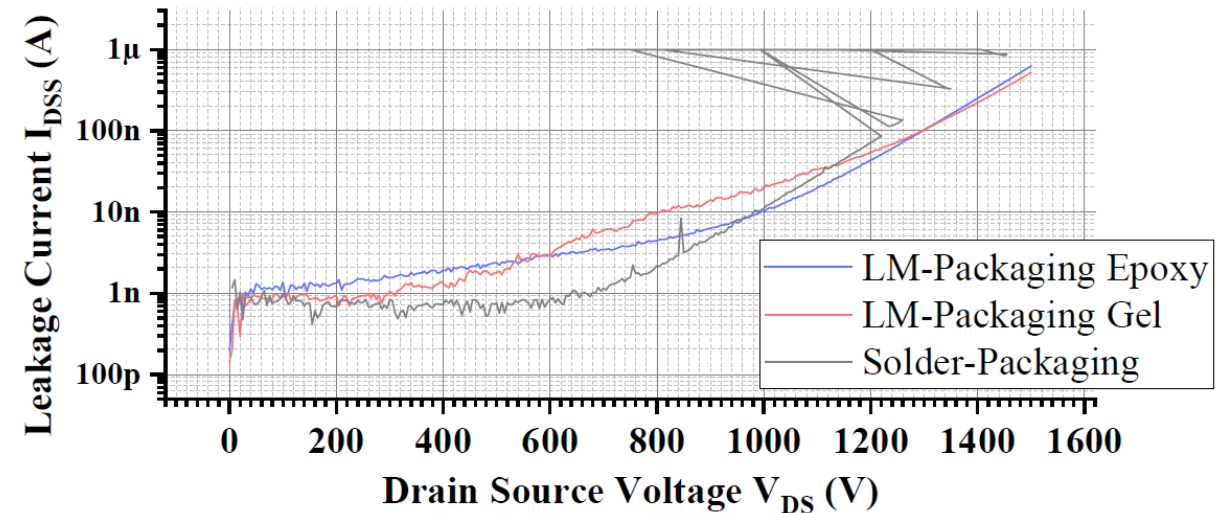
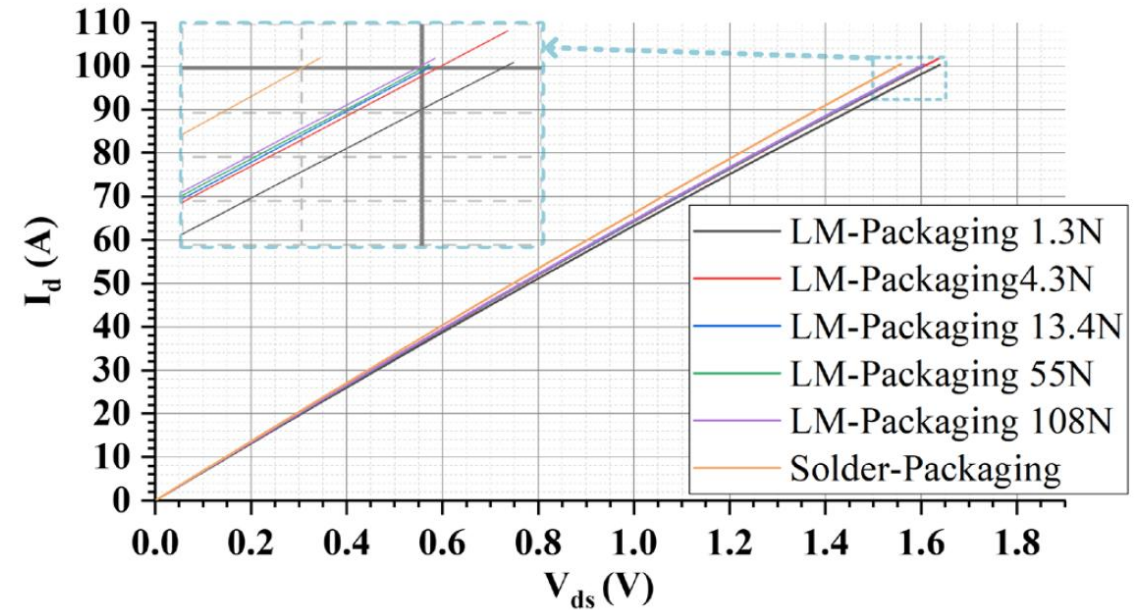
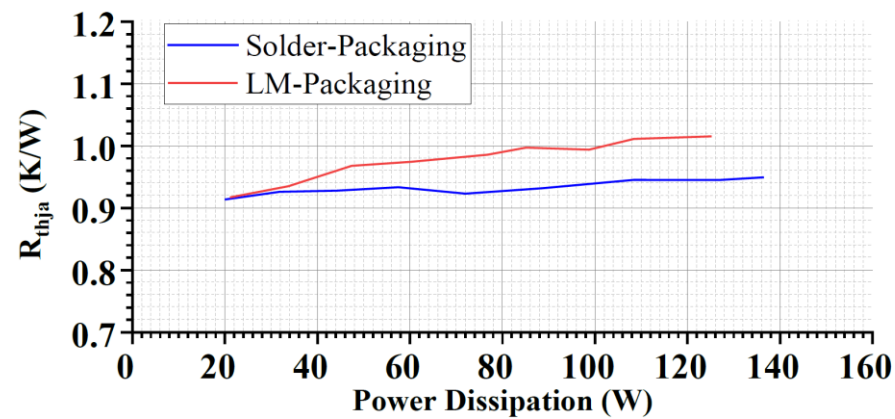
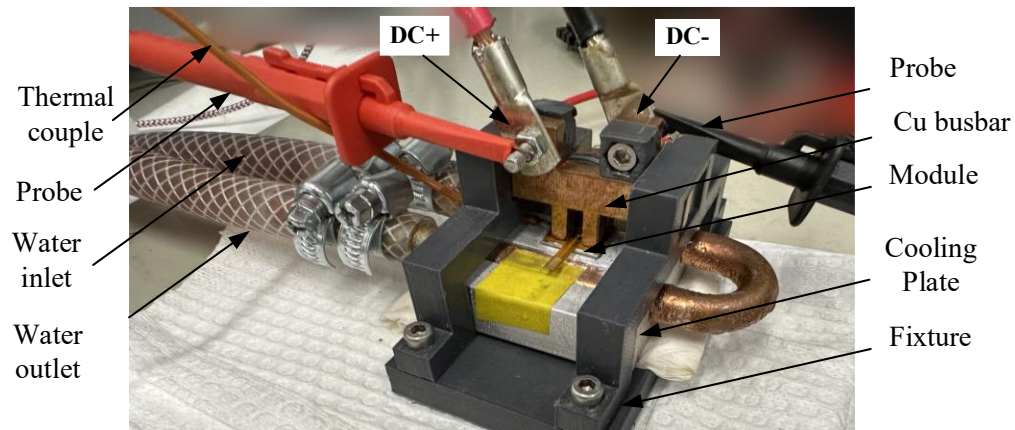
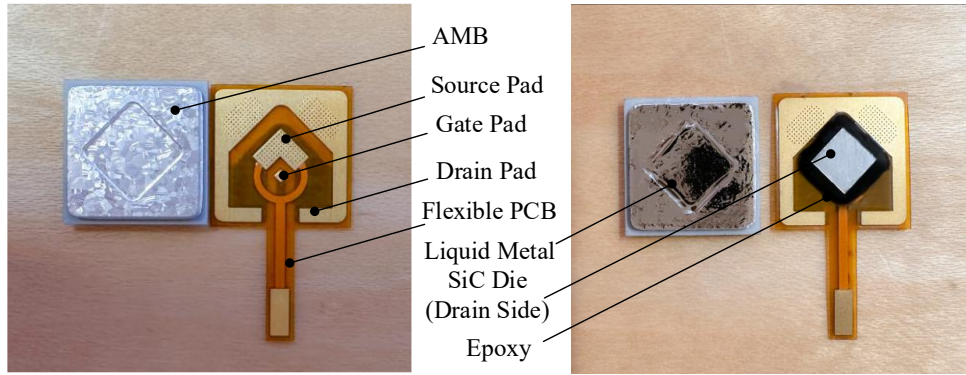
- ❖ Shear stress comparison of the AMB
- 99% reduction of surface share stress.



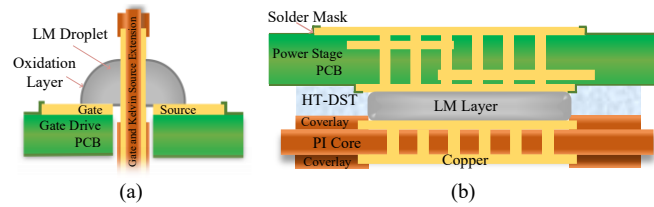
(a) Conventional Solder Module (b) Liquid Metal Module

- ❖ Shear stress comparison of the FPCB
- Improved reliability for FPCB

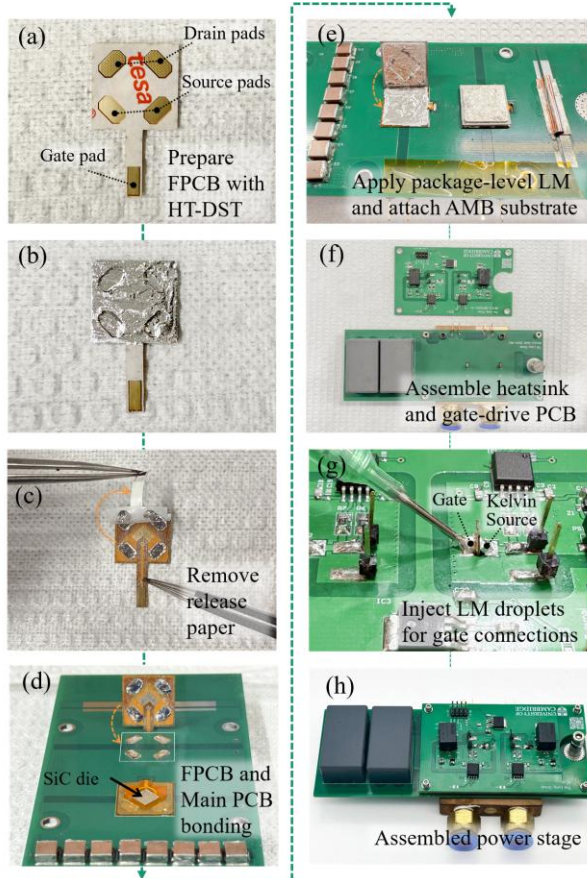
Excellent thermal and electrical conduction using LM in packaging



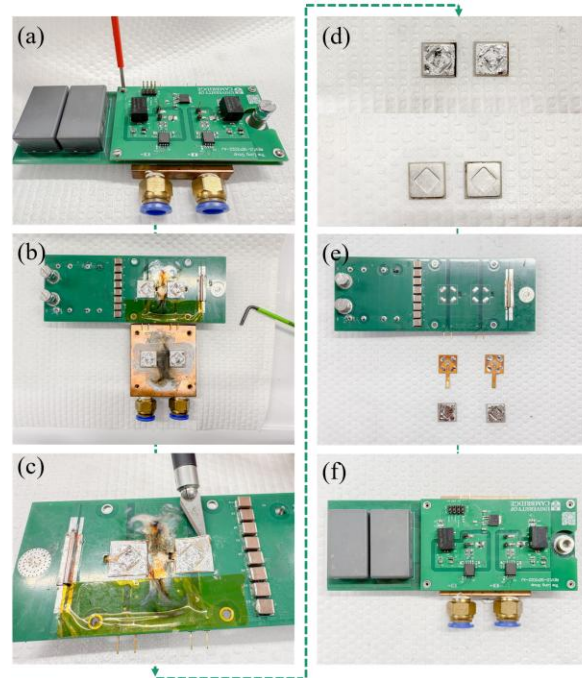
Repairable, Recyclable, and Reliable Power Electronics



Using Liquid Metal (LM) for components' connection to PCBs



Process of LM based PCB assembling

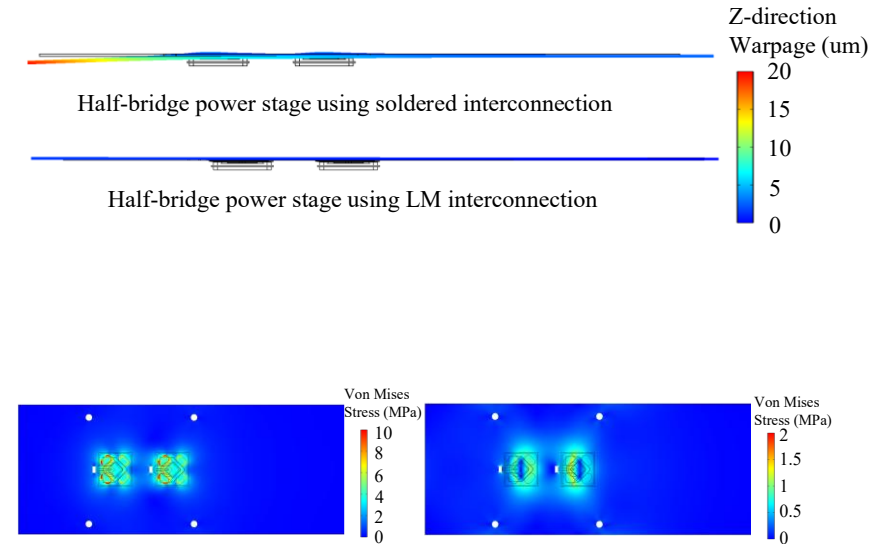


Straight forward **Repairing/Replacing** failed SiC device package enabled by LM converter PCB assembly design

Working progress:

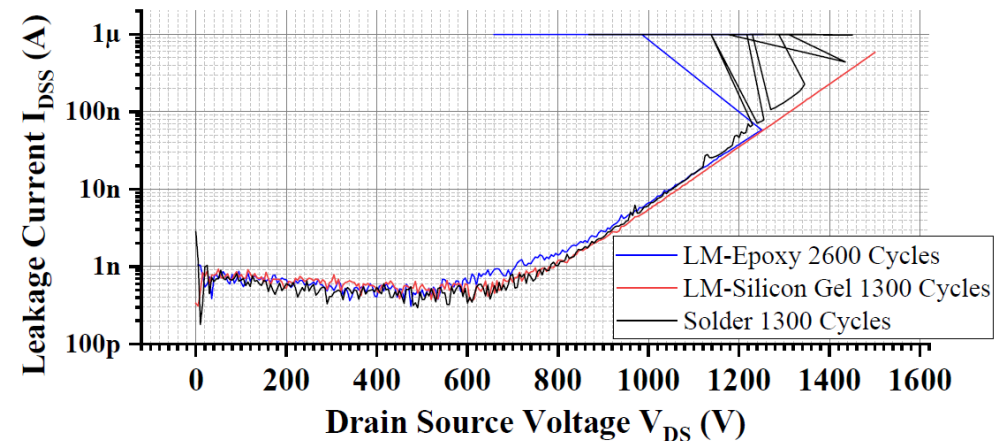
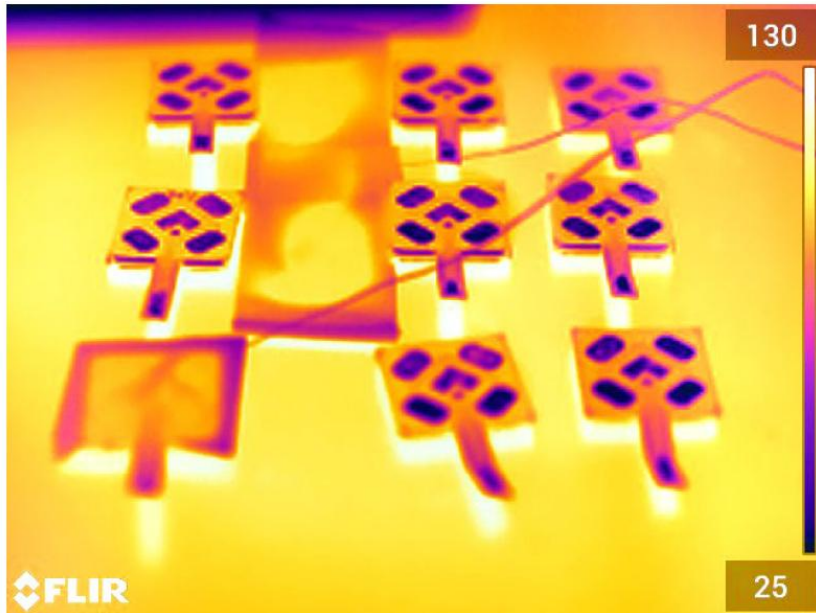
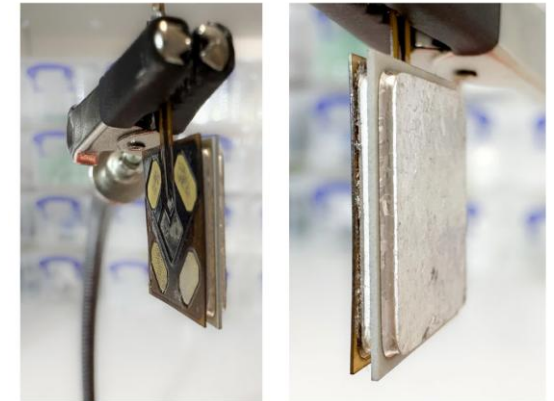
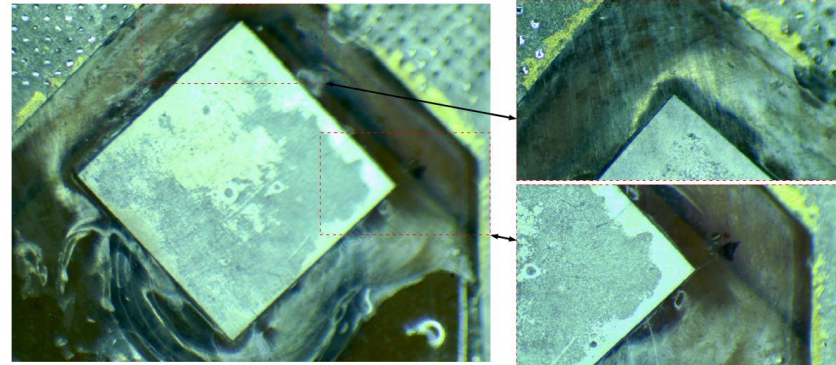
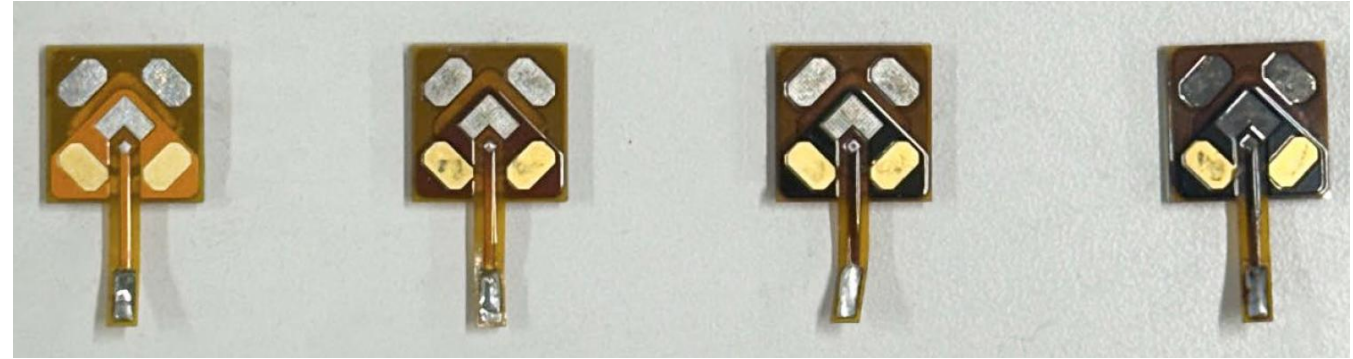
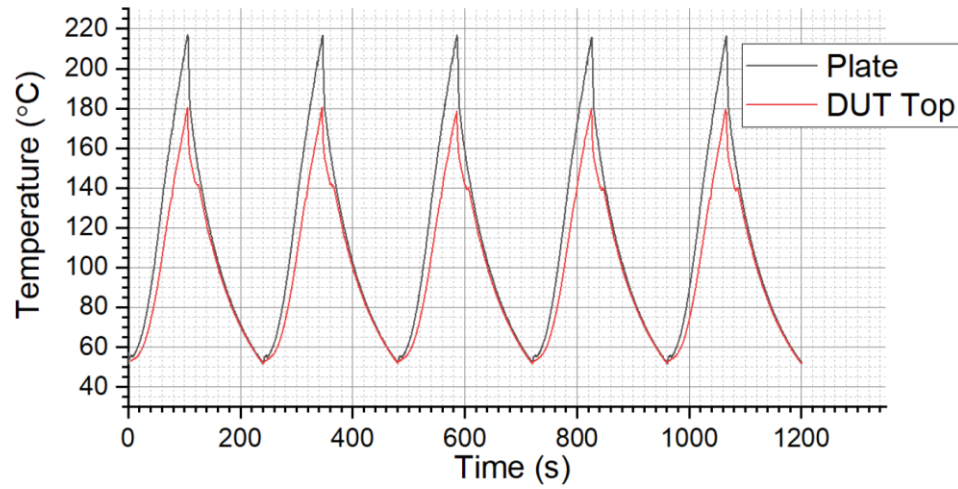
- Corrosion of LM (GaInAg) to copper and silver needs to be investigated, particularly with power device metallization (12 month).
- Power cycling tests of entire PCB assembly will be conducted (9 month).
- One paper submitted to IEEE Trans on Power Electronics (under review).

W. Mu, A. Janabi, B. Hu, L. Shillaber and T. Long, "Liquid Metal Fluidic Connection and Floating Die Structure for Ultralow Thermomechanical Stress of SiC Power Electronics Packaging," in *IEEE Transactions on Power Electronics*, vol. 39, no. 7, pp. 7808-7814, July 2024,

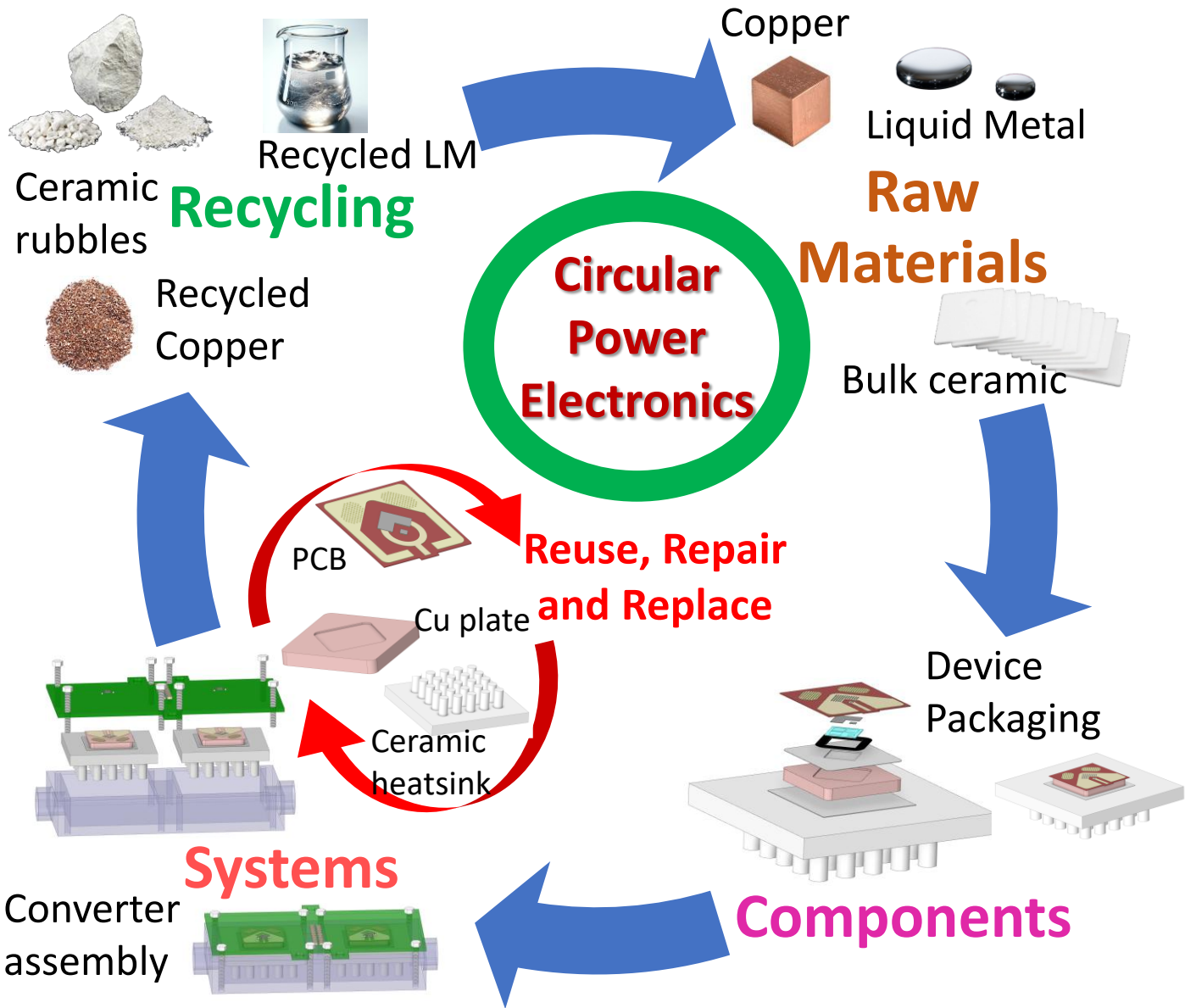


Significant thermomechanical stress reduction increasing **reliability** of the converter PCB assembly

Temperature cycling shows consistence of LM and damming



Circular Power Electronics



UK Research and Innovation

[Home](#) [Applications](#) [Reviews](#) [Panels](#)

Funding Service

BETA This is a new service – your [feedback](#) will help us to improve it.

[Back to Application](#)

APP32215: Advanced Device Packaging Enabling High Performance and Circular Power Electronics (CircularPE)

Resources and costs

Total full economic cost (fEC)	Total funding applied for	Total contribution from applying organisations
£1,339,731	£1,071,784.80	£267,946.20

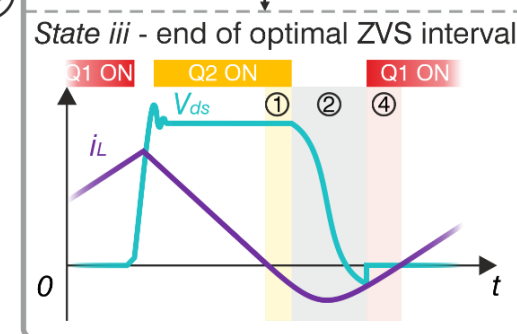
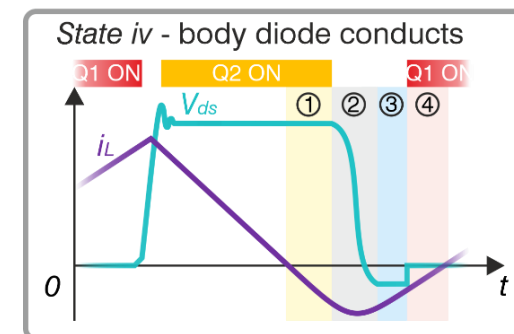
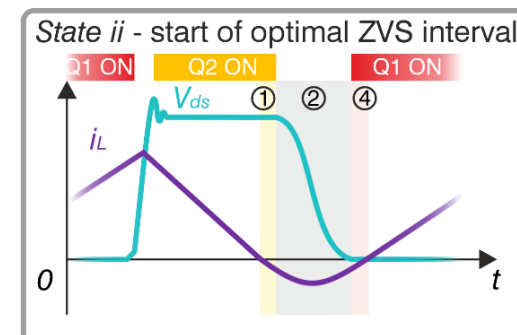
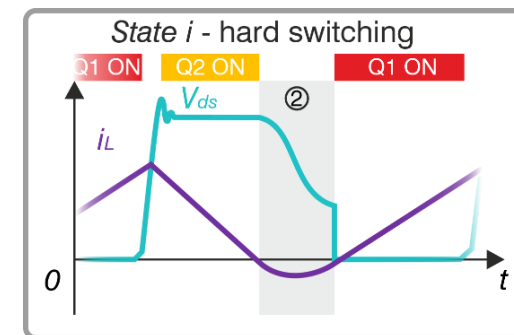
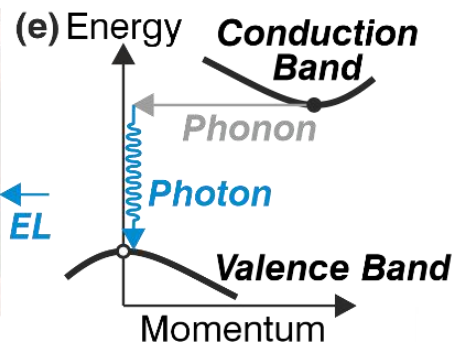
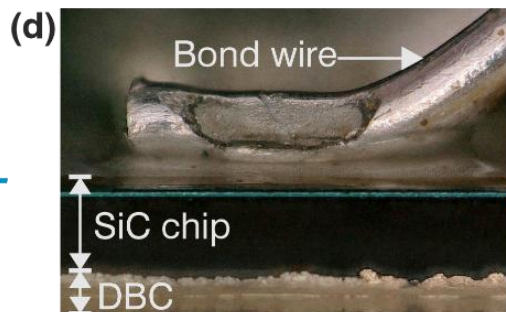
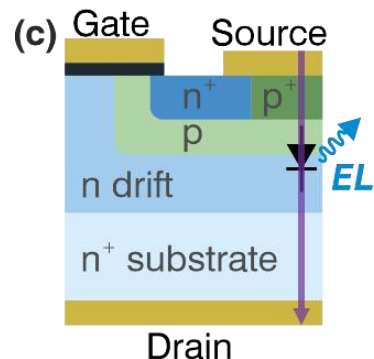
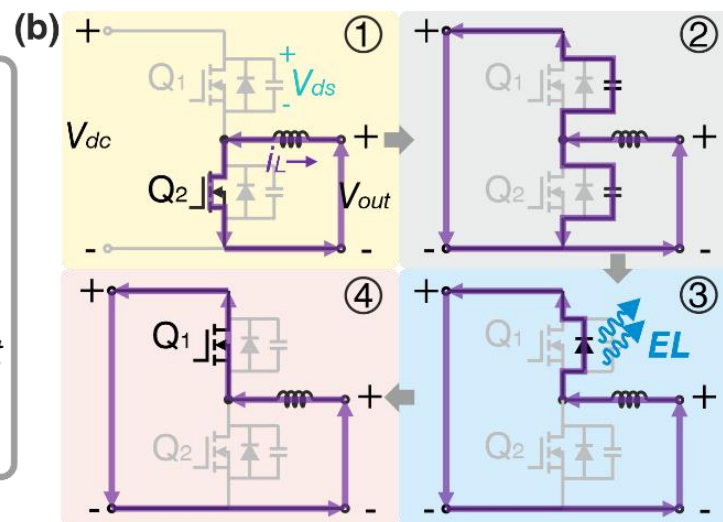
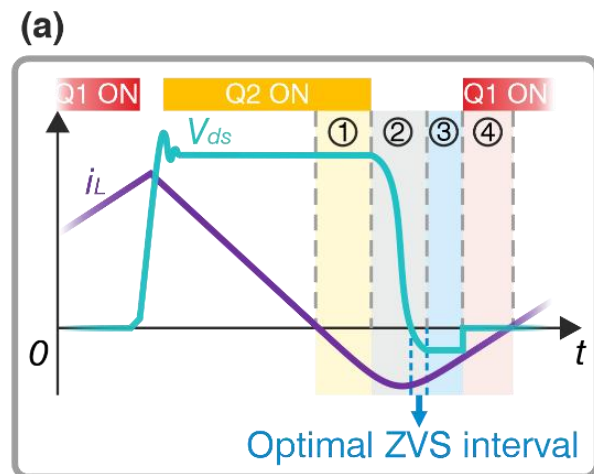
Add resources and costs for each organisation

Organisation	Full economic cost (fEC)	
University of Cambridge	£841,277	Complete ✓
Compound Semiconductor Applications Catapult	£498,454	Complete ✓

Contents

- State-of-the-art Power Supply Architecture for AI datacentres
- Advanced Power Electronics Packaging for for High Integration
- Smart Soft-Switching using Electroluminescence

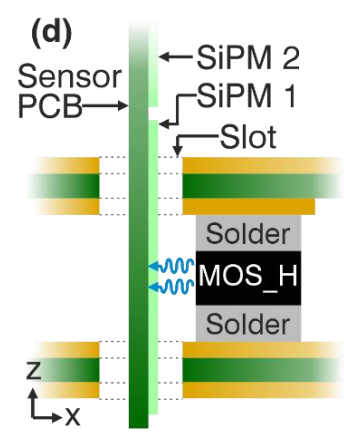
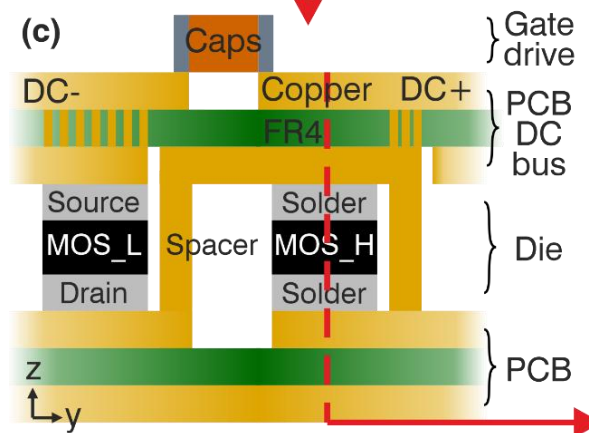
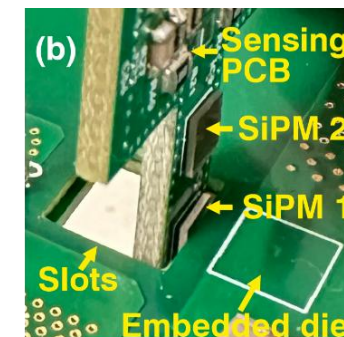
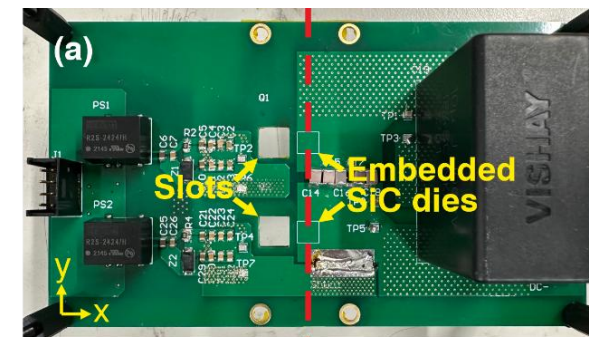
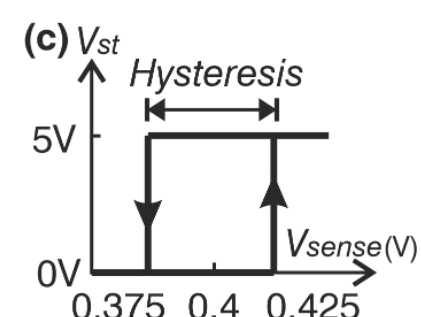
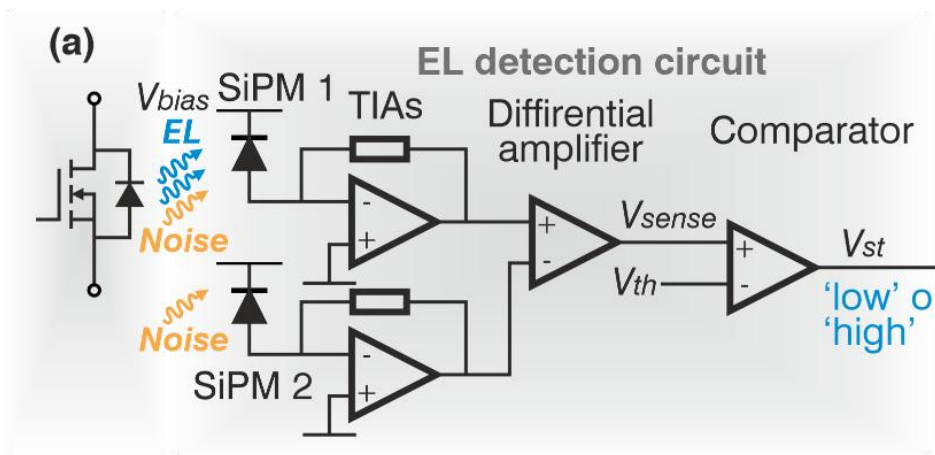
Optically Triggered Self-Adaptive ZVS



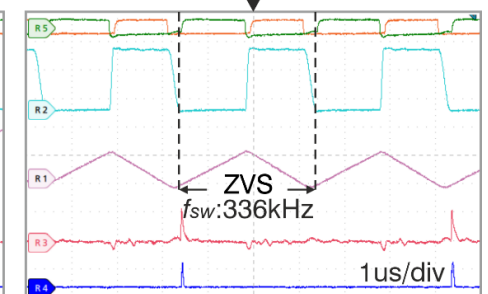
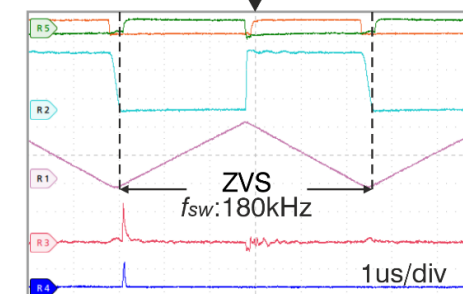
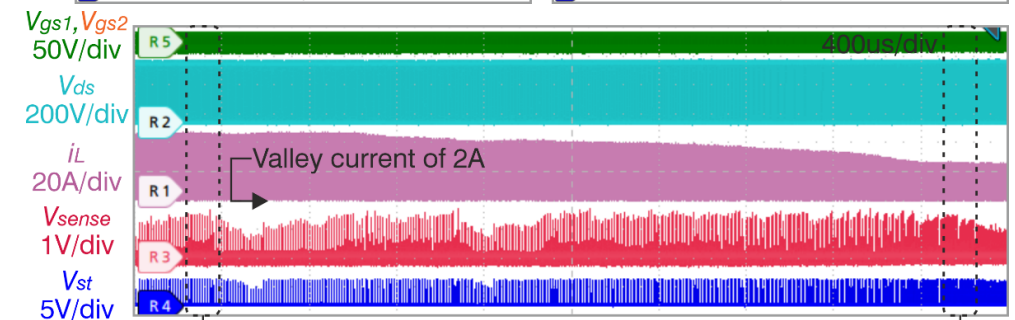
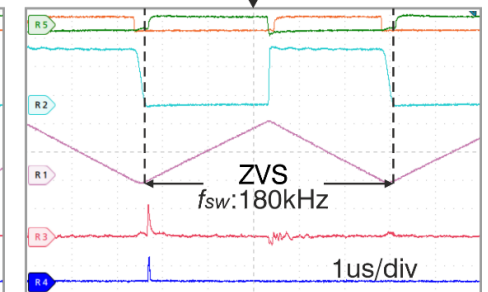
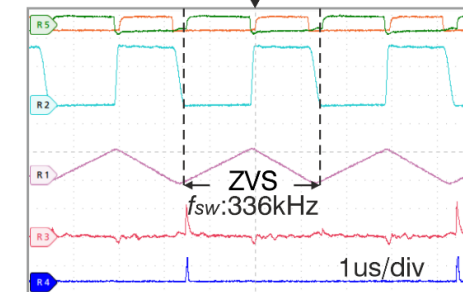
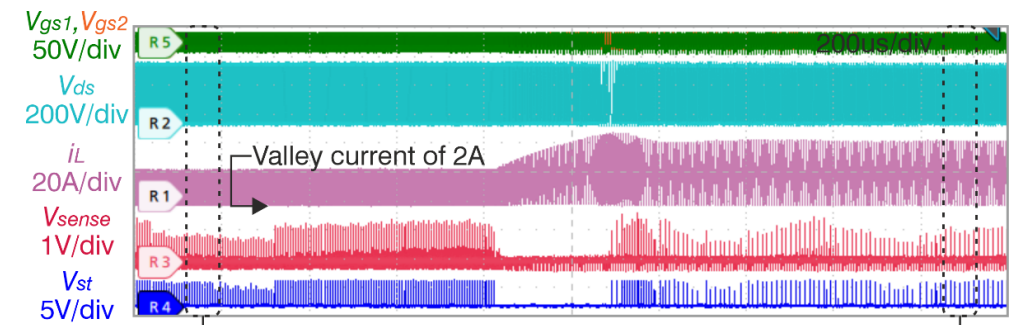
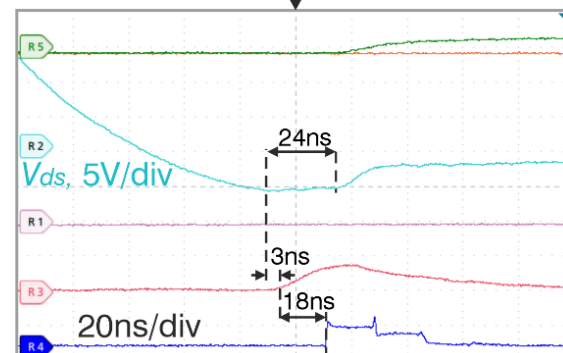
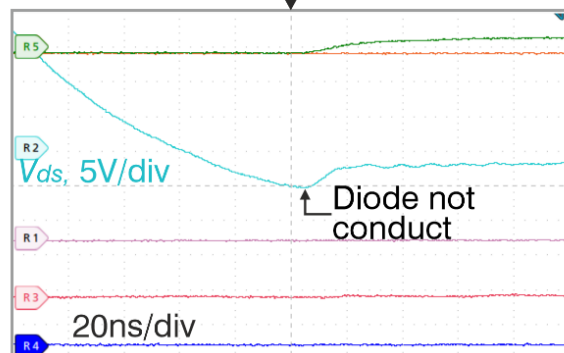
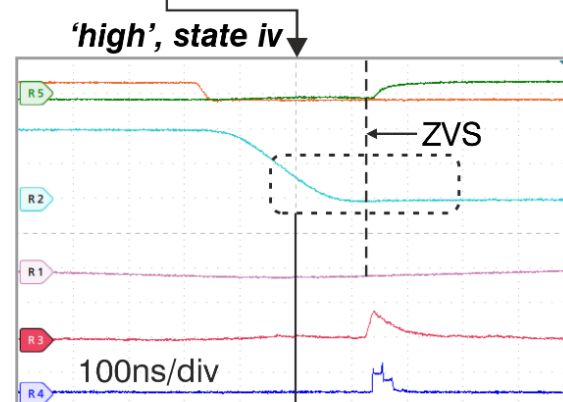
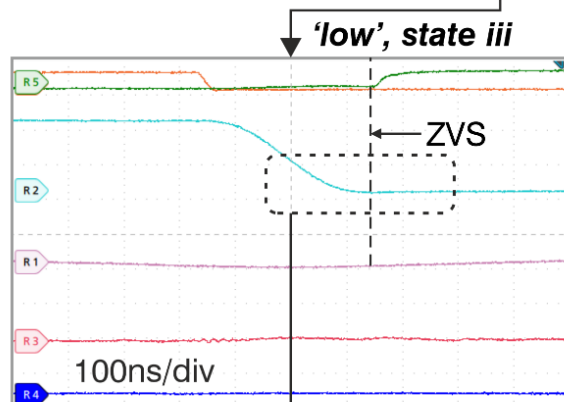
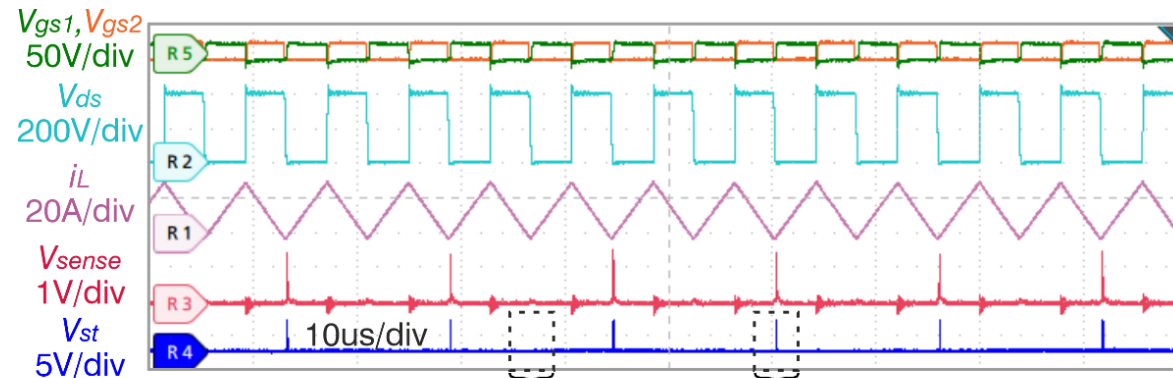
Diode conducts, EL detected, $f_{sw,n+1} = f_{sw,n} + \Delta f_{sw}$
 Diode not conduct, $f_{sw,n+1} = f_{sw,n} - \Delta f_{sw}$



Experimental validation



Results



Cambridge Power Electronics Laboratory (The Long Group)



Prof Teng Long
Chair of Power Electronics

The Long Group

Packaging	Converter	System
Embedding & Integration	AC-DC DC-DC	Transport Electrification
Packaging Materials	Switching & Soft Switching	Server/Datacenter Power Supplies
Modelling & Reliability	Magnetics & Inductive Device	Sustainable Power Electronics



Engineering and
Physical Sciences
Research Council



Innovate
UK



UNIVERSITY OF
CAMBRIDGE

AI Power Demands Make Power Electronics **Great Again**

