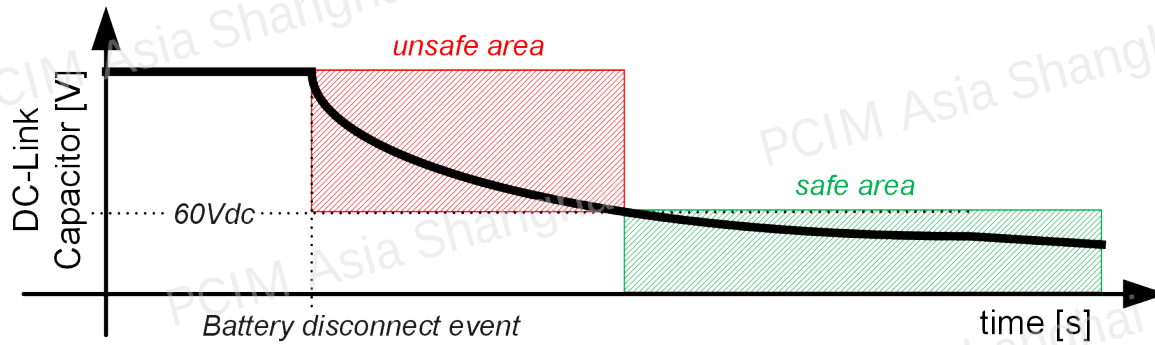
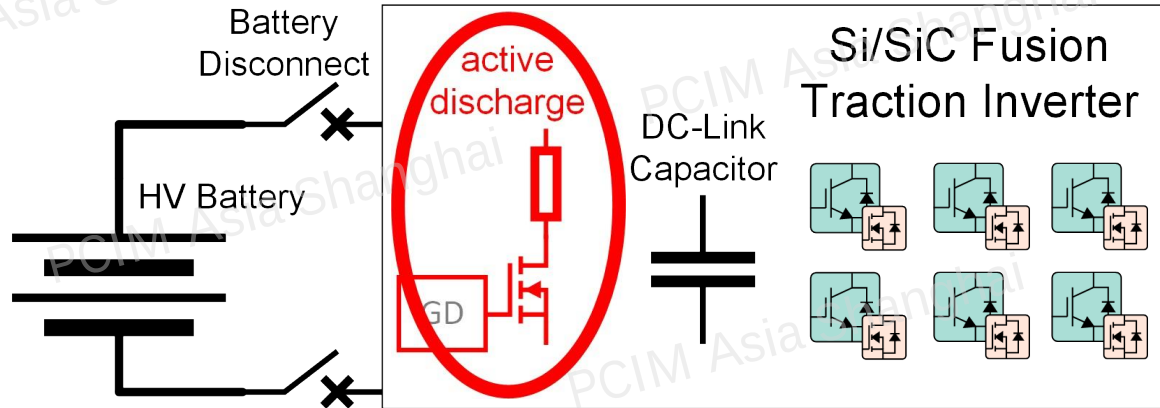


Active DC-Link capacitor discharge methods with Si/SiC Fusion power module for addressing vehicle cost down

Tomas Reiter, J. Schapdick, M. Krug, M. Weinmann, M. Niendorf
Infineon Technologies AG

Active DC-Link capacitor discharge

Motivation and Key Requirements



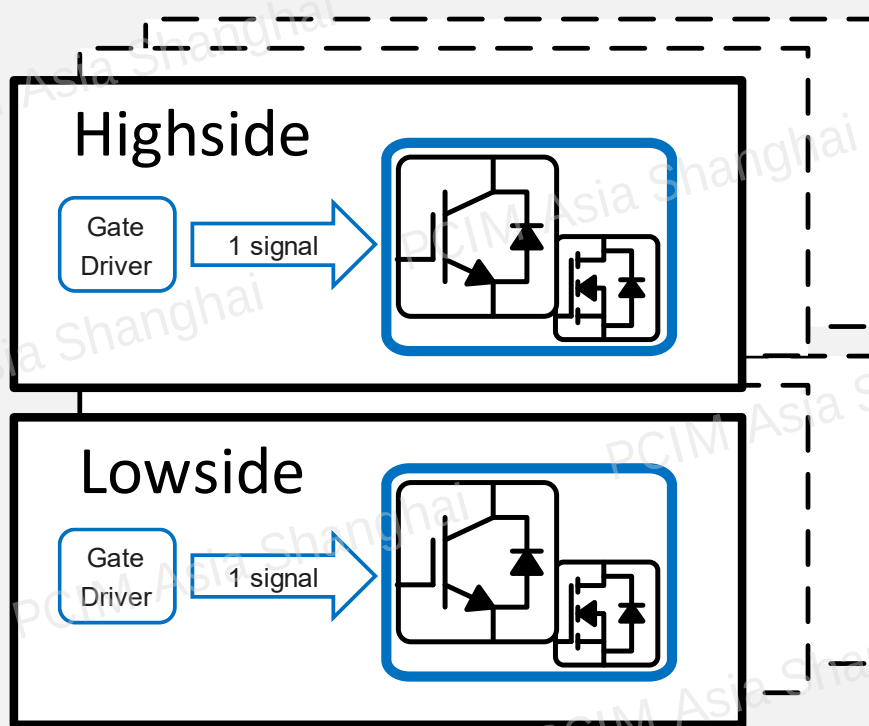
- ISO 6469-4:2015 electric safety requirements
- The DC-link capacitor must be discharged to below 60 V_{DC} within 5 seconds.
- Target: No additional switches/resistors/snubbers
=> use of the existing inverter power electronics!
- Energy to discharge at each event:
 - $E_D = \frac{1}{2} \cdot C_{DCL} \cdot (V_{DC1}^2 - V_{DC2}^2)$
 - With 1mF capacitor at 500V => 123 Joule
- Lifetime to consider:
 - 15 years each day minimum 2x discharge event.
 - $E_{D_lifetime} = 2 \cdot 365 \cdot 15 \cdot E_D = 1.35 \text{ Mega Joule}$

Si/SiC Fusion switch for Active Discharge

Challenge to distribute Active Discharge load

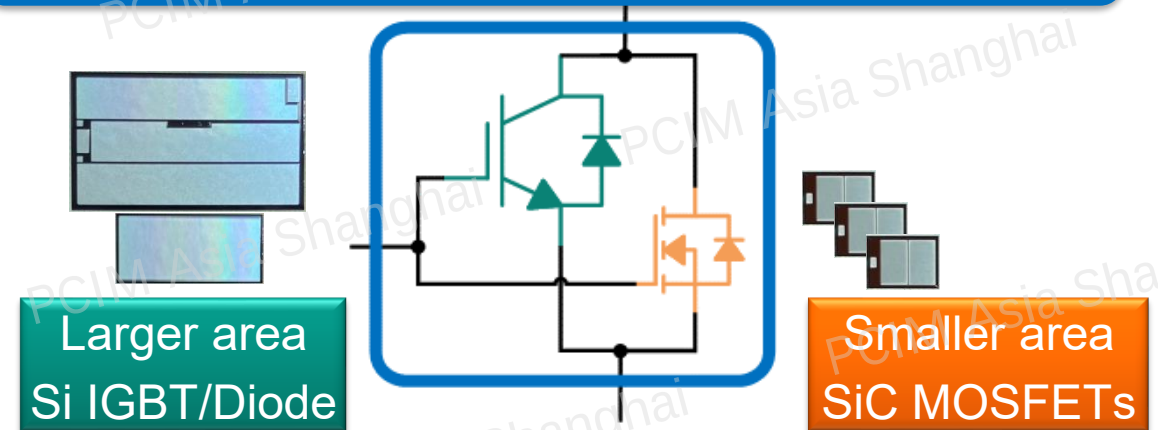
Fusion Switch: Optimized for „Single Gate Drive“

3 Phases



- Single Gate drive leaves no possibility to directly control current share rate.
- SiC has smaller area. Efficiency for light load.
- IGBT has large die area. Carry high currents.

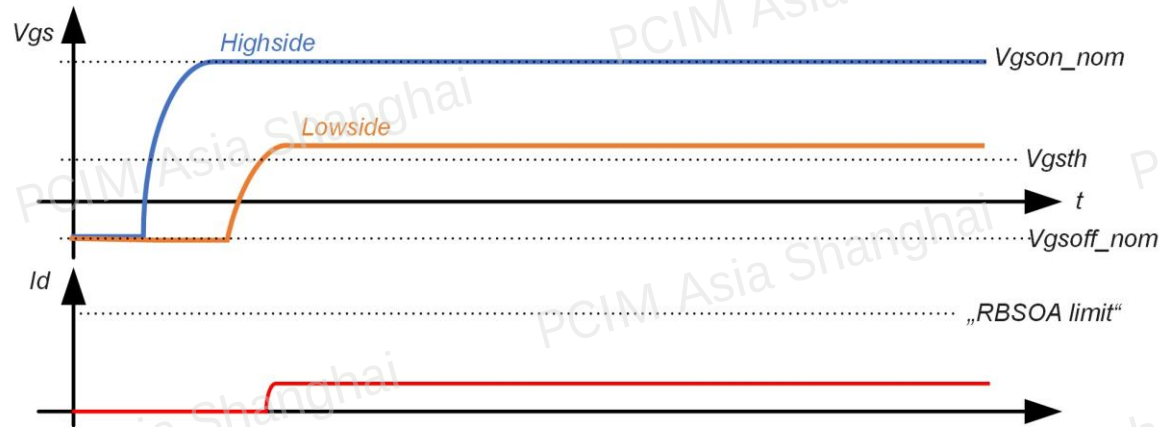
Si/SiC Fusion switch („3 Terminal Device“)



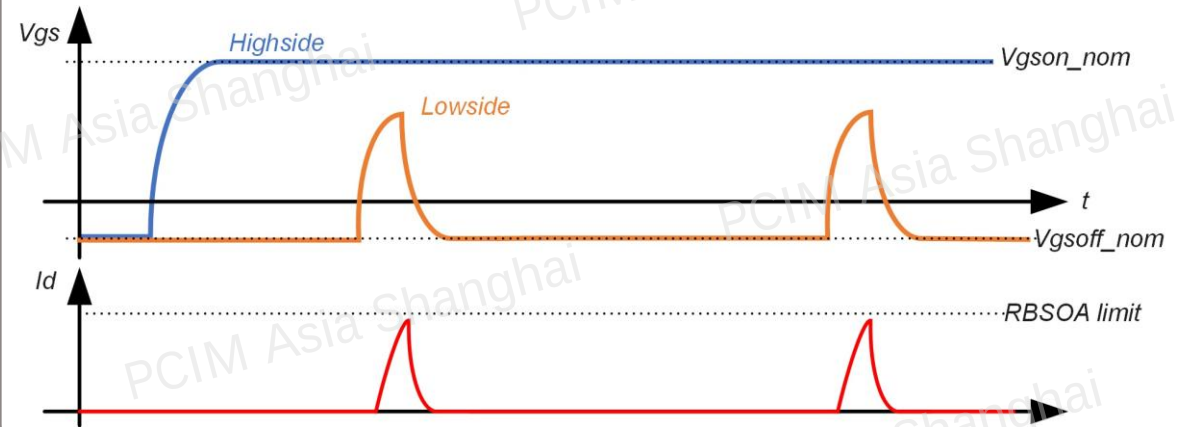
Challenge: How to distribute the active discharge load proportional to the die sizes on Si IGBT and the smaller SiC MOSFET!

Active DC-Link capacitor discharge Methods under Investigation

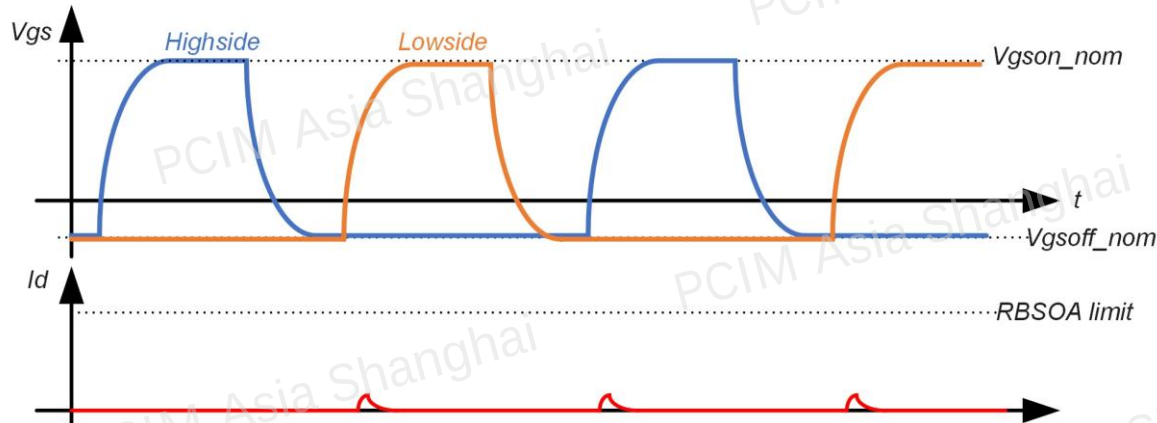
1) Linear Mode



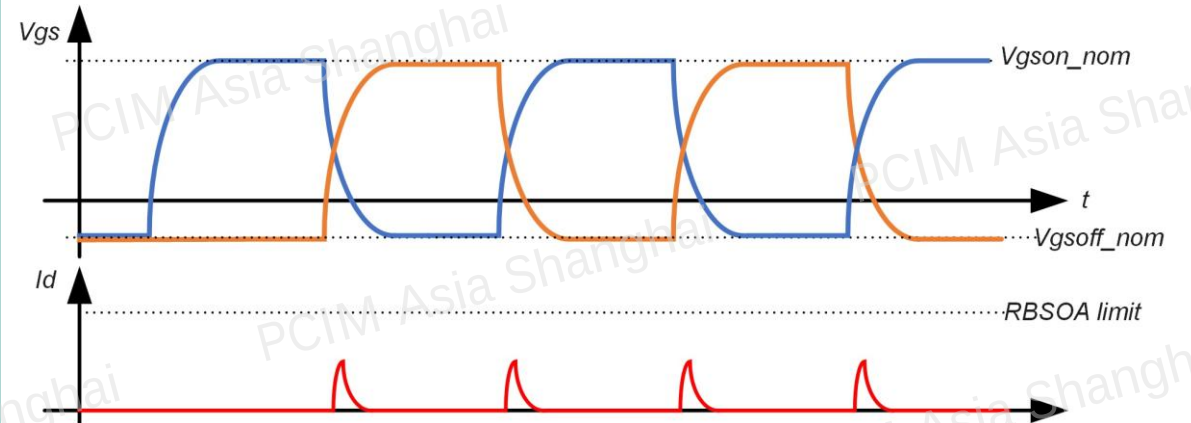
2) „Weak turn-on short circuit“



3) PWM discharge by IGBT Coes & MOSFET Coss

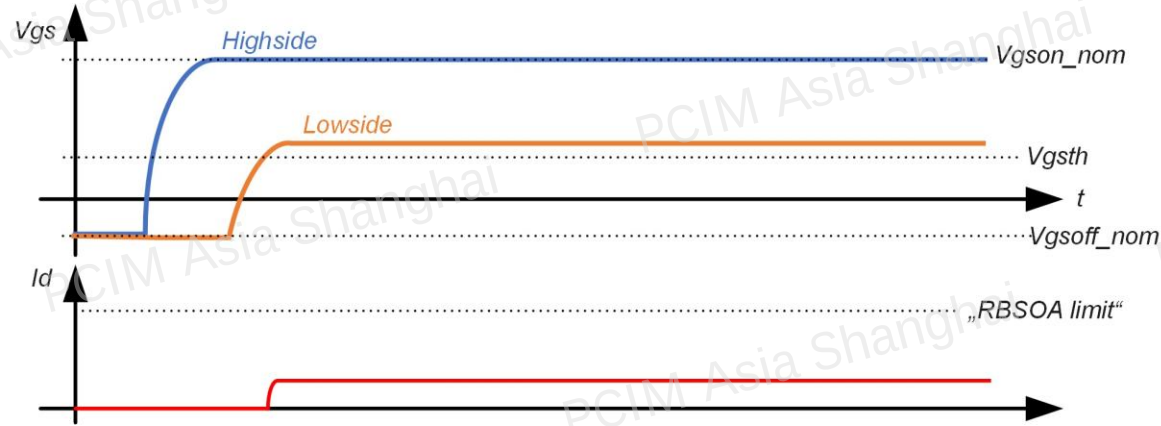


4) PWM discharge with controlled overlap



Active DC-Link capacitor discharge with Si/SiC Fusion Switch

1. Linear Mode

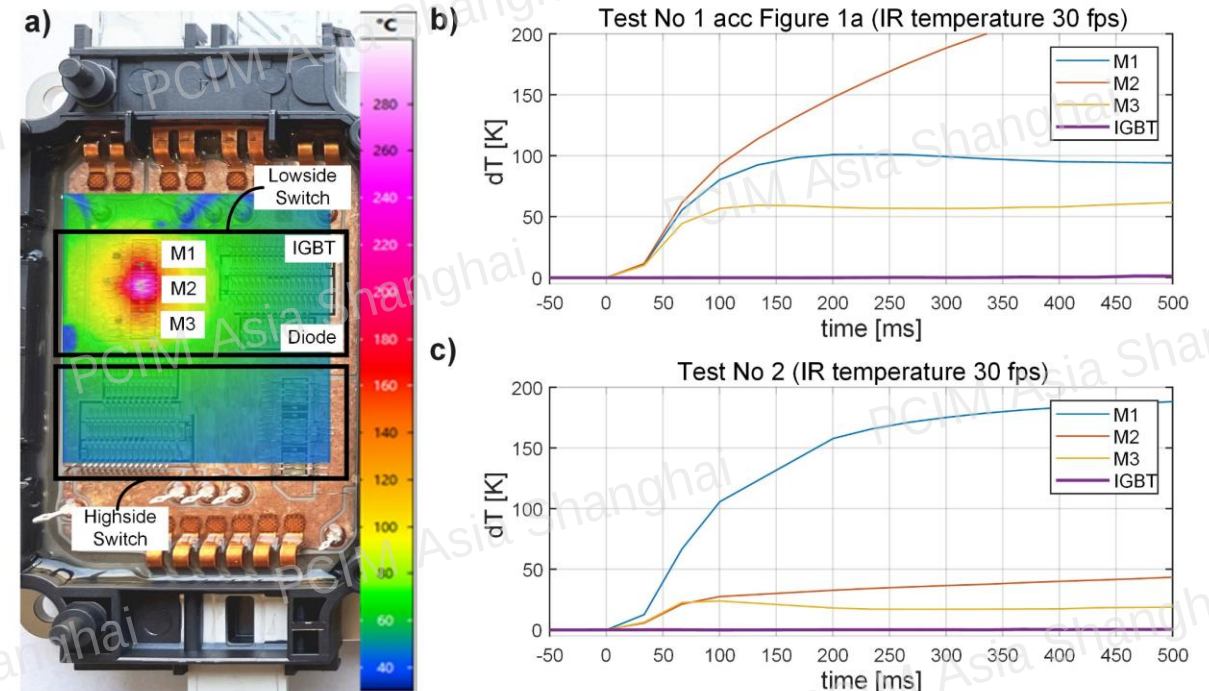


Aspects to consider for Si/SiC Fusion „Linear Mode“

- SiC MOSFET $V_{gs_{th}} < \text{IGBT } V_{geth}$.
 - SiC MOSFET designed with small die area.
 - AECQ and AQC324 do not consider testcoverage of linear mode operation.
- Both, SiC MOSFET and IGBT are not specified and tested for linear mode.

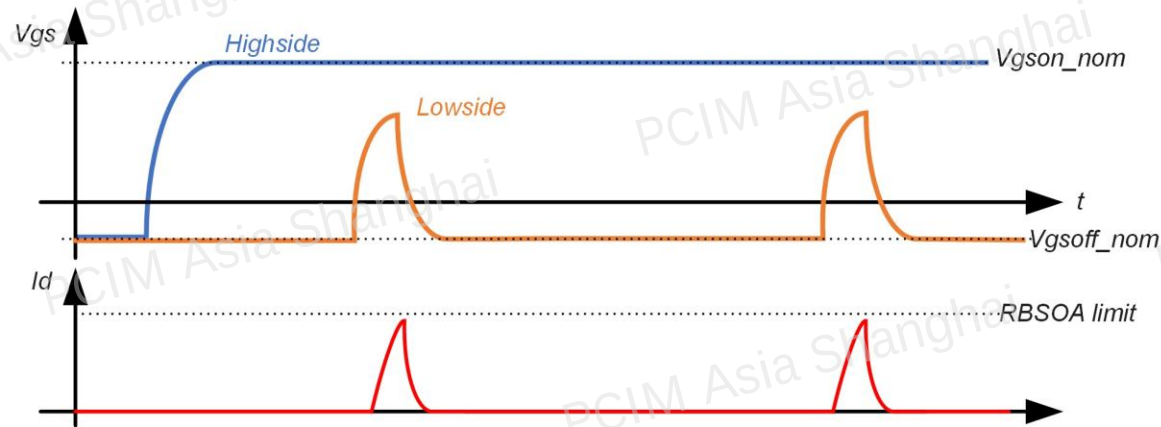
Experimental Results with Si/SiC Fusion switch

- Unpredictable thermal stress.
 - Each part and condition behaves different.
 - Not within scope of specifications.
- **Method has high risk! To be avoided where possible!**



Active DC-Link capacitor discharge with Si/SiC Fusion Switch

2. Weak turn-on short circuit (WTO SC)

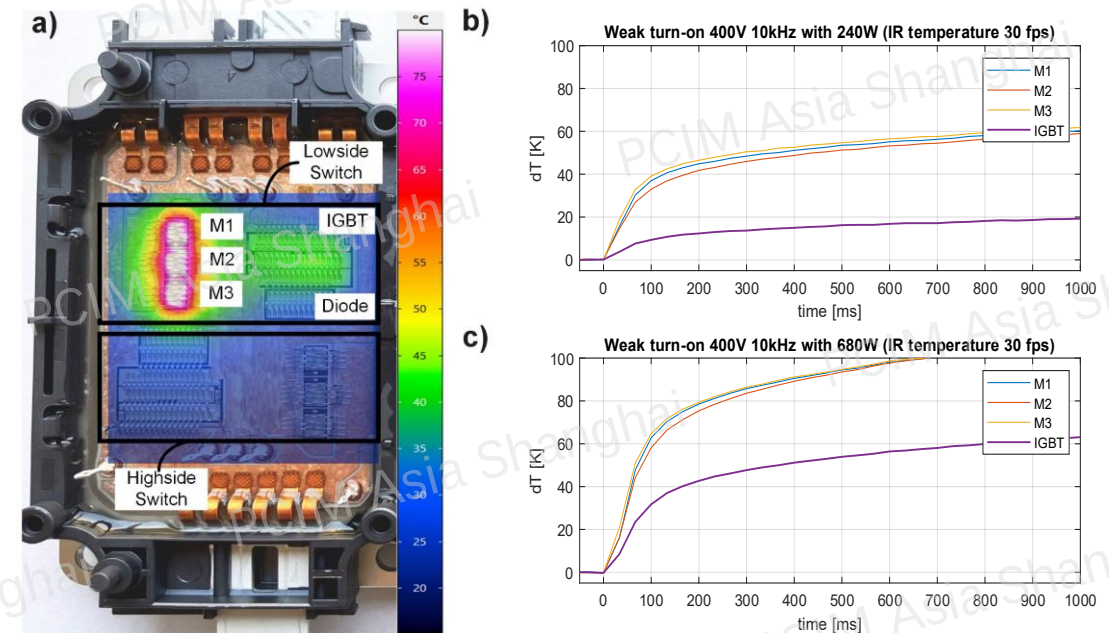


Aspects to consider for Si/SiC Fusion „WTO SC“

- Si/SiC Fusion switches can be designed short circuit robust. See also DOI: [10.30420/566262369](https://doi.org/10.30420/566262369)
- SiC MOSFET $V_{gsth} < IGBT V_{geth}$.
- Pulse duration must be extreme short due to fast switching behavior.

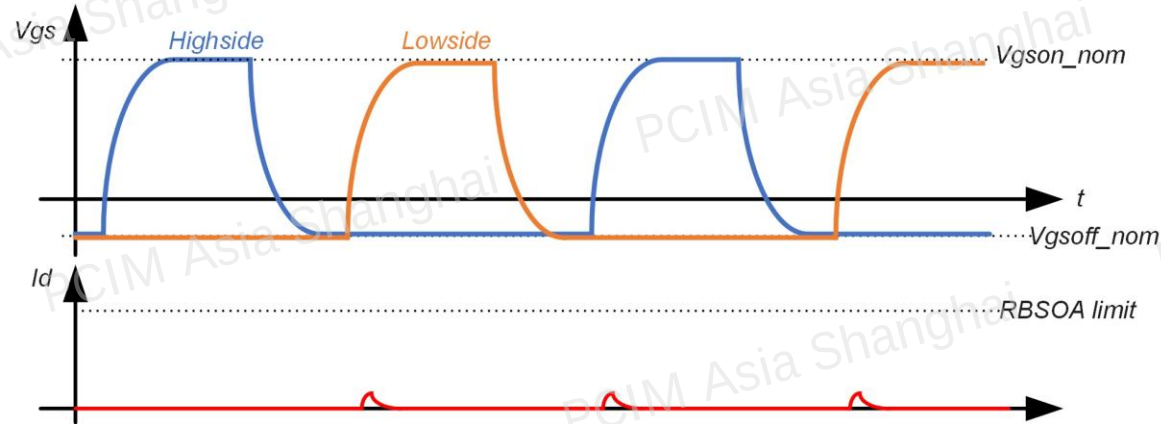
Experimental Results with Si/SiC Fusion switch

- Suitable pulse duration window was only 30 ns (t_{pulse} from 130 to 160 ns).
- At high currents the IGBT start to contribute.
- A balanced IGBT/SiC stress condition was not achievable.



Active DC-Link capacitor discharge with Si/SiC Fusion Switch

3. PWM discharge by IGBT Coes & MOSFET Coss

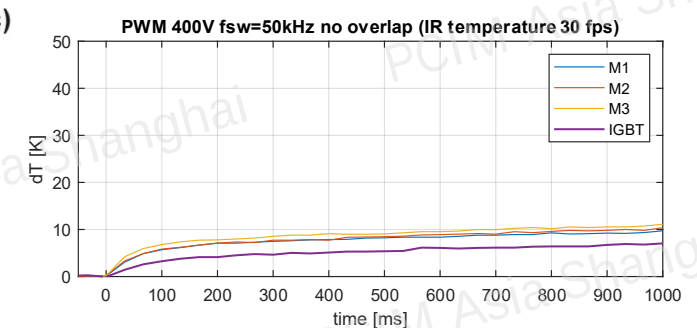
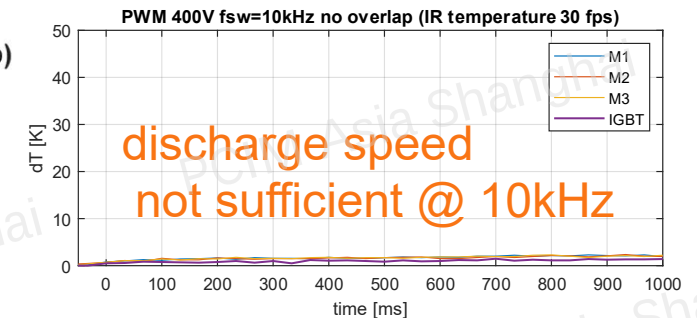
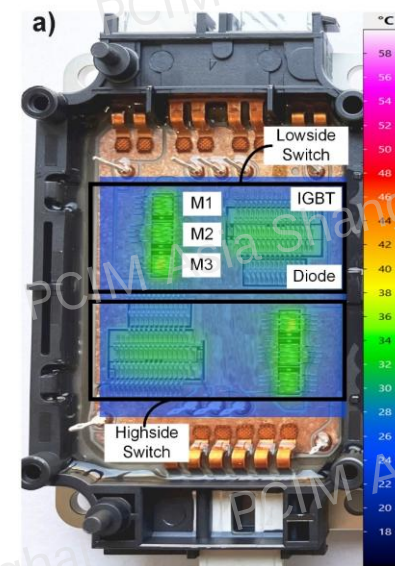


Experimental Results with Si/SiC Fusion switch

- A good option with balanced power device stress.
- 10 kHz will not provide enough discharge speed.
- Needs overdimensioning of gate drive power supplies to ensure $f_{sw} = 50...100$ kHz!

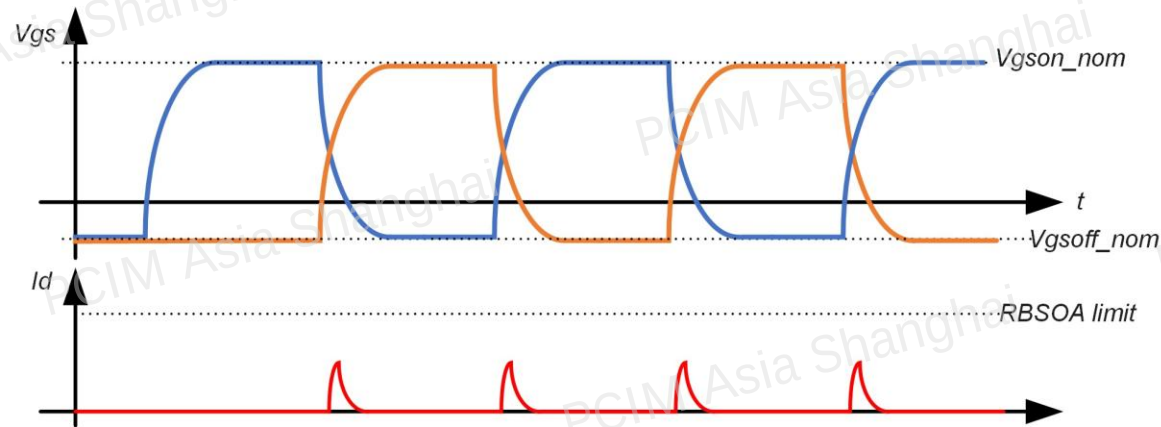
Aspects to consider for Fusion „Coes|oss discharge“

- Both output capacitances C_{oes} and C_{oss} has to be designed low (light-load efficiency inverter operation).
- Switching frequency 10..100 kHz is OK for the Fusion switch itself.
- Typical traction inverter gate drive power supply will be designed for $f_{sw} \leq 20$ kHz operation.



Active DC-Link capacitor discharge with Si/SiC Fusion Switch

4. PWM discharge by „Controlled Overlap“

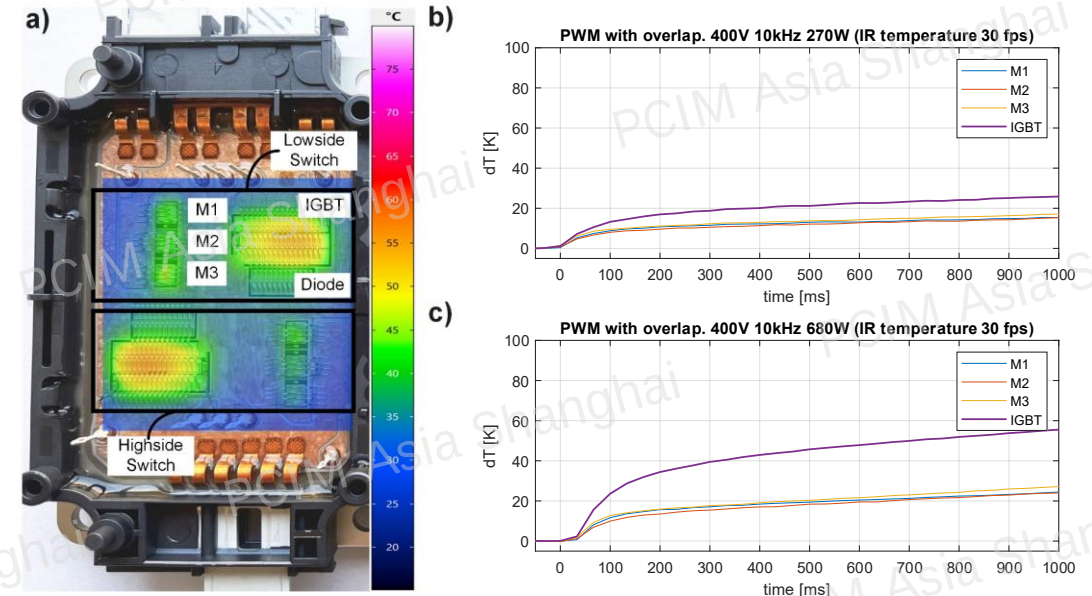


Experimental Results with Si/SiC Fusion switch

- Stable discharge conditions.
- IGBT/SiC stress is „self-balanced“
 - Low currents $\Rightarrow$ SiC MOSFET with small die area
 - High currents $\Rightarrow$ IGBT with larger die area

Aspects to consider for Fusion „Overlap discharge“

- A transient shoot-through is not critical as long it is not „too long“.
- One switch dissipate turn-on energy (mainly SiC) where the complementary switch dissipate turn-off energy (mainly IGBT).



Active DC-Link capacitor discharge with Si/SiC Fusion Switch

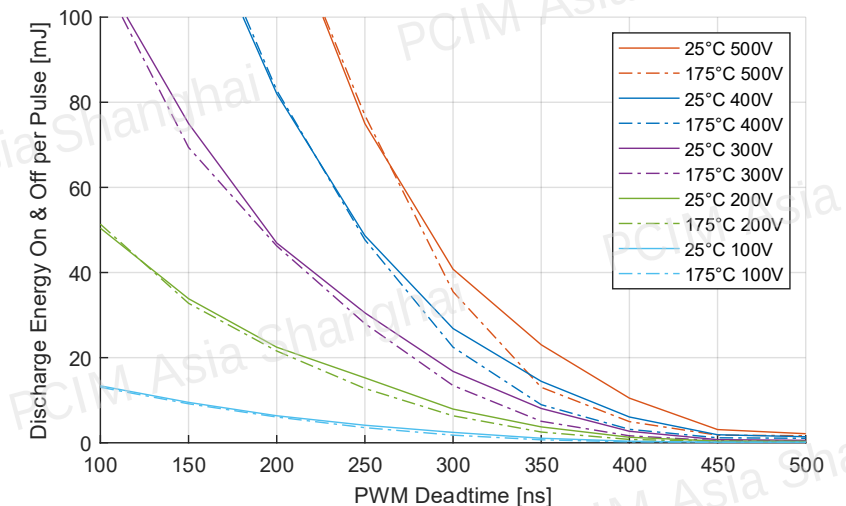
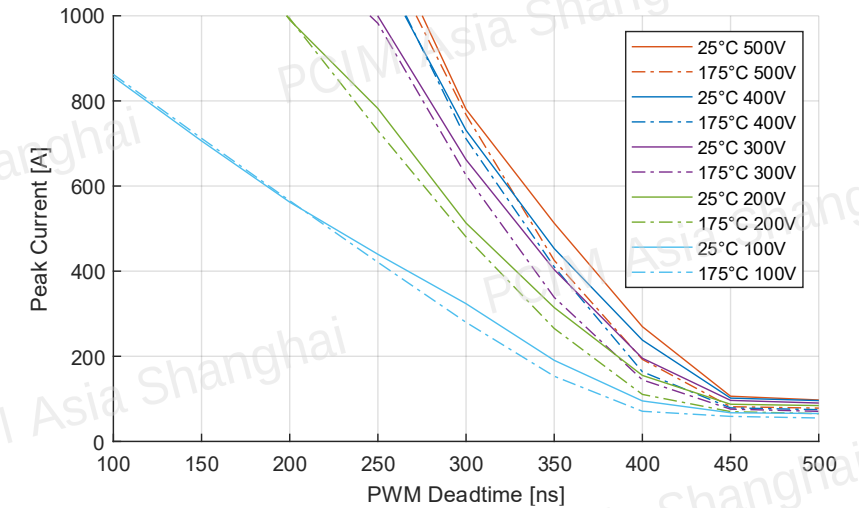
4. PWM discharge by „Controlled Overlap“

Key Findings of Si/SiC Fusion in „Controlled Overlap“

- The PWM signal dead time where overlap begins is stable over voltage & temperature.
- The „start point“ is also stable over part-to-part tolerances: $R_g \cdot C_{ies}$ for Fusion is lower compared to only IGBT or full SiC solutions.
- Dead time need to be adjusted during discharge to ensure sufficient discharge speed:
 - e.g., 350..400ns dead time needed @500V
 - e.g., 150..200ns dead time needed @100V

Challenge & Motivation:

Discharge method should work robust without any sensor feedback.



Active DC-Link capacitor discharge with Si/SiC Fusion Switch

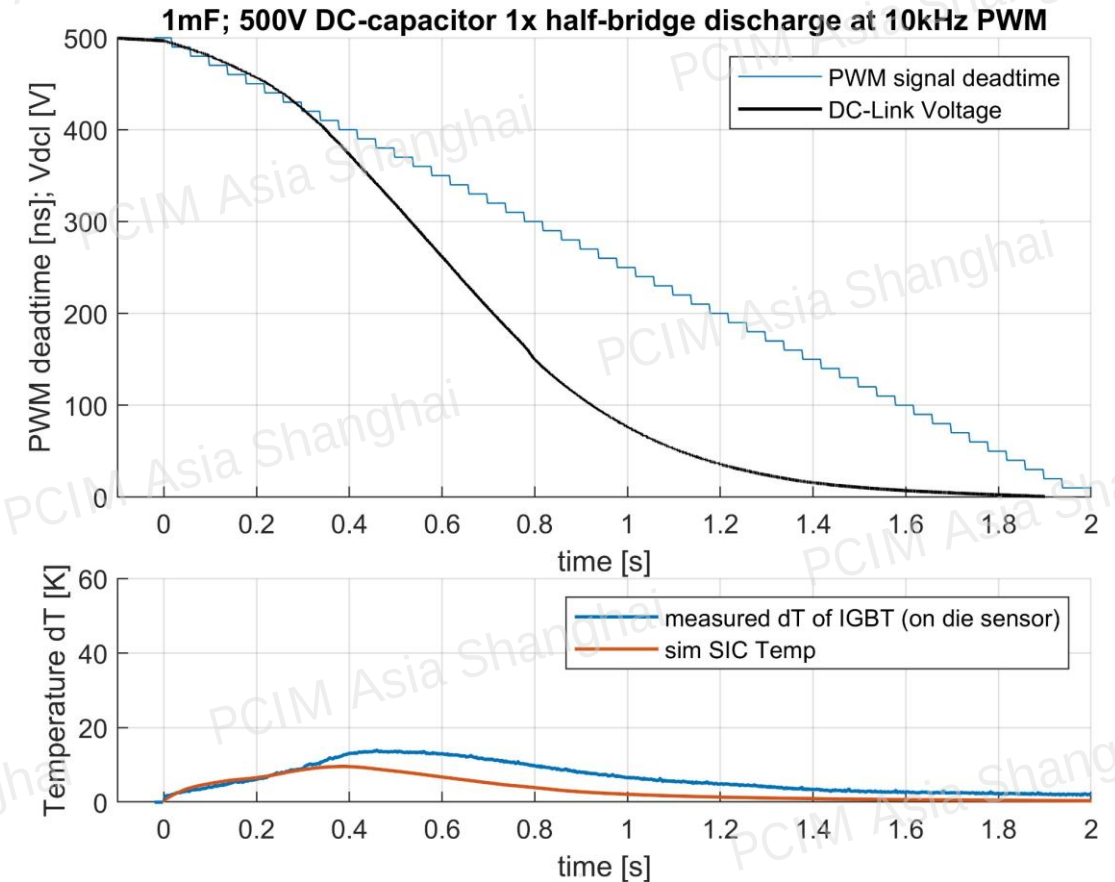
4. PWM discharge by „Controlled Overlap“

Robust Discharge Approach:

- A simple linear PWM dead time ramp can solve the problem.
- Low peak currents during discharge achieved $< 0.5 \times \text{RBSOA limit}$.
- Low ΔT of the power switches ($< 20\text{K}$).



The measurement was done
- Without coolant fluid
- Only one half bridge



Remaining Question:

Any device degradation to expect?

Active DC-Link capacitor discharge with Si/SiC Fusion Switch

4. PWM discharge by „Controlled Overlap“

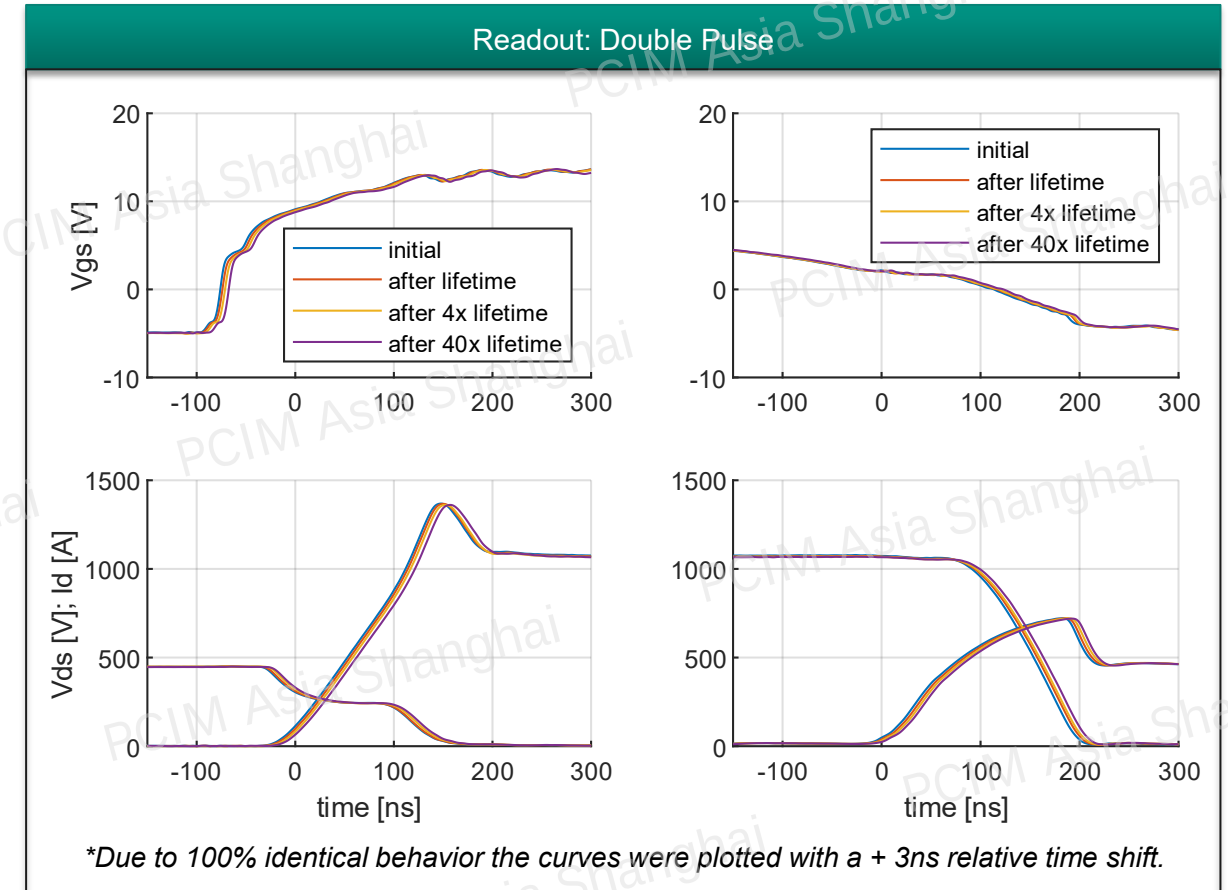
Method:

- Double Pulse Readout
- Stress Test (11k cycles capacitor discharge)
- Double Pulse Readout



Stress Test Condition:

- 1000 μF Capacitor charged at 500V
- Start Temperature: $T_{vj} = 150^{\circ}\text{C}$
- Discharge on Single Phase-Leg
- 11 kcycles of capacitor discharge (i.e. 15y lifetime)



Result: No lifetime degradation from discharge method

Active DC-Link capacitor discharge with Si/SiC Fusion Switch

Conclusion

Active DC-Link discharge via the Si/SiC Fusion power module	Linear mode	Weak Turn-on SC	PWM Coss, Coes discharge	PWM controlled overlap
Discharge time <5 s with fsw < 20 kHz	✓	✓	✗	✓
Active short circuit can be maintained	✓	✓	✓	✓
DESAT short circuit detection active	✗	✓	✓	✓
Shoot-through protection active	✗	✗	✓	✓
Balanced stress IGBT/SiC	✗	✗	✗	✓
Balanced stress Highside and Lowside	✗	✗	✓	✓
Device stress covered by std specification and reliability testing	✗	✗	✓	✓

Key Findings

- 1) „Controlled overlap“ discharge method fits best to Si/SiC Fusion switches.
- 2) Device Stress between IGBT/SiC is „Self-Balanced“.
- 3) No consumption of „Lifetime“ observed.

Thank you for attending the presentation.
 Any Questions?

Paper on Si/SiC Fusion:

Switching Behavior / Calorimetric Measurements



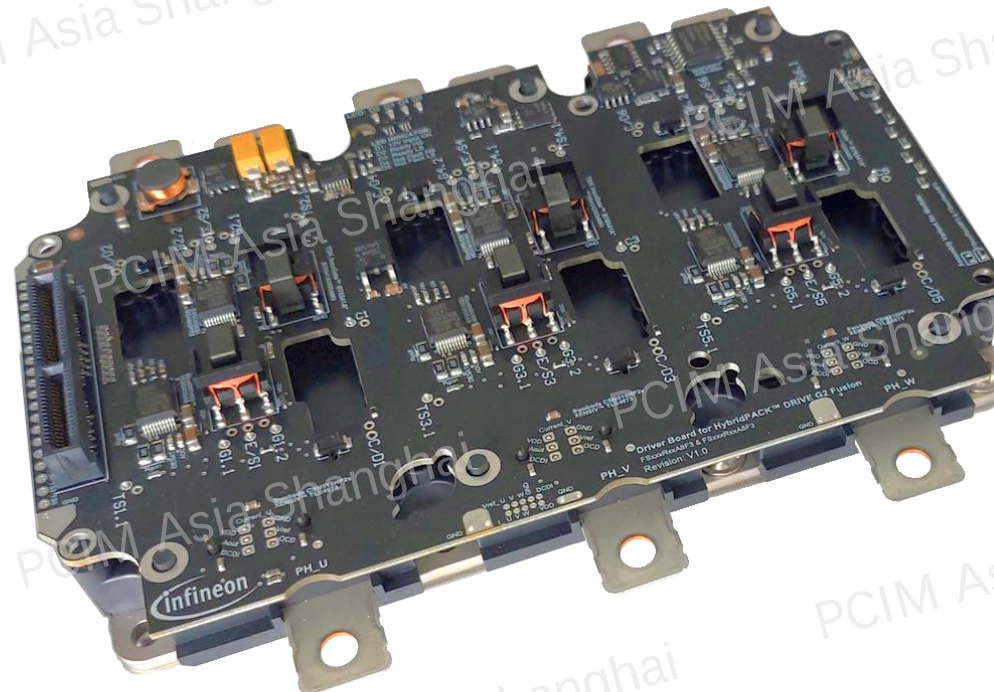
[Fusion switch concept addresses the cost-performance dilemma in EV powertrains](#)

Paper on Si/SiC Fusion:

Vehicle Benefits / Cost Comparison



[Benefits of Si/SiC Fusion Switch for EREV Architectures](#)



Si/SiC Fusion Power Module Evaluation Kit (open design files)