pcim
ASIA SHANGHAI

Topic： “PowerChiplet” Technology, Ultra-high-power Density Platform for Future Power Electronics

Chair: Naoto Fuiishima, Fuii Electric,JP

Organizer： Ichiro Omura， Kyushu Institute of Technology, JP

Conference Room 1

Topic：
“PowerChiplet” Technology, Ultra-high-power Density Platform for Future Power Electronics

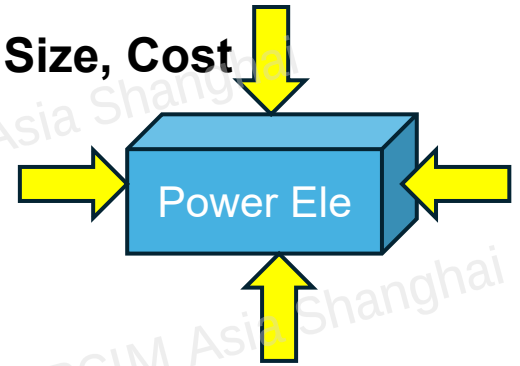
Chair: Naoto Fuiishima, Fuii Electric,JP
Organizer：Ichiro Omura, Kyushu Institute of Technology, JP

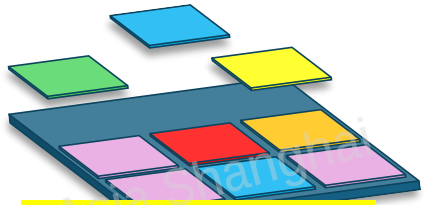
Motivation

Achieving higher power density has been a key issue in power electronics, driven by the increasing demand for miniaturization in AI servers, powertrains, and on-board chargers (OBCs) for electric vehicles (EVs). However, **a next-generation platform for future ultra-high-power-density power electronics has not yet been clearly defined**.

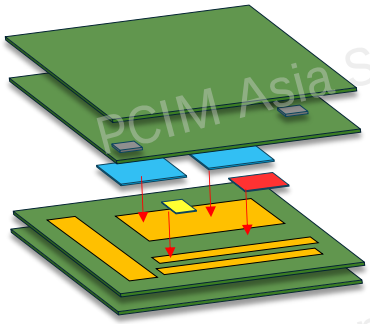
In **high-performance computing (HPC), "Chiplet"** technology has emerged as a future platform to address the **slowdown of Moore's Law**, **reduce costs**, and enable advanced heterogeneous integration. This concept is expected to be adopted in power electronics to achieve ultra-high-power density and a high level of system integration.

In this session, the new concept of the **"PowerChiplet"** will be discussed for the first time as a **future platform for power electronics**, with **a focus on chip-embedded PCB technology**. The speakers are specialists from China, Japan, and Europe. If you are interested in the future impact of "Power Chiplet" concept in power electronics as the ultra-high power density platforms, and system integration with chip embedded PCB technology, we invite you to join this session.



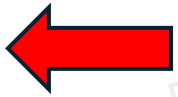


Chiplet for HPC



Power Chiplet?

Presentations

- **Power Chiplet Technology for Next Generation Power Electronics Systems**
  Speaker: Ichiro Omura, Kyushu Institute of Technology, JP
- **Advanced Packages With Power-On-Substrate Solutions**
  Speaker: **Frye Fung**, Zhuhai ACCESS Semiconductor Co., Ltd.. CN
- **Chip Embedded Panel level Power Package for AI and Vehicles**
  Speaker: **Yoshiaki Aizawa**, Aoi Electronics, JP
- **Novel Integration Concepts for Power Electronics - Embedding of SiC MOSFET for High-performance Power Modules**
  Speaker: **Lars Boettcher**, Fraunhofer IZM Berlin, DE
- **Discussion** 

Power-Chiplet Technology for Next Generation Power Electronics Systems

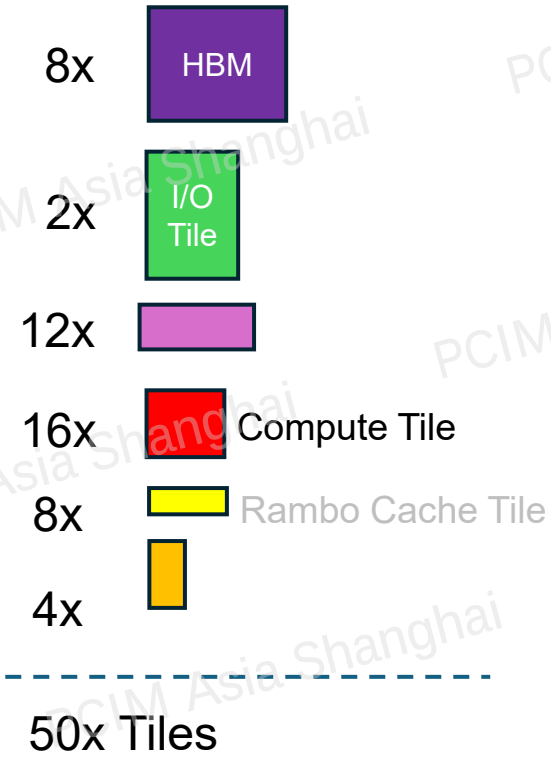
Ichiro Omura
Kyushu Institute of Technology
Japan
大村 一郎　九州工业大学

Agenda

- "Chiplet" for High Performance Computing
- Road Maps of Power Semiconductors
- Why “PowerChiplet”?
  - Chip level
  - Gate drive / Circuit level
  - System level
- Summary

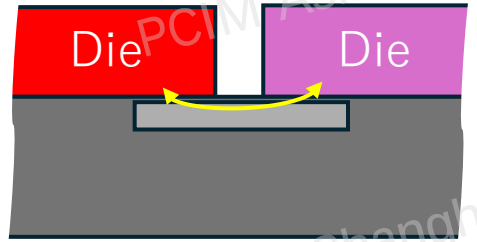
Chiplet, how it looks like?

Tiles of Different Nodes



Intel Ponte Vecchio GPU

EMIB



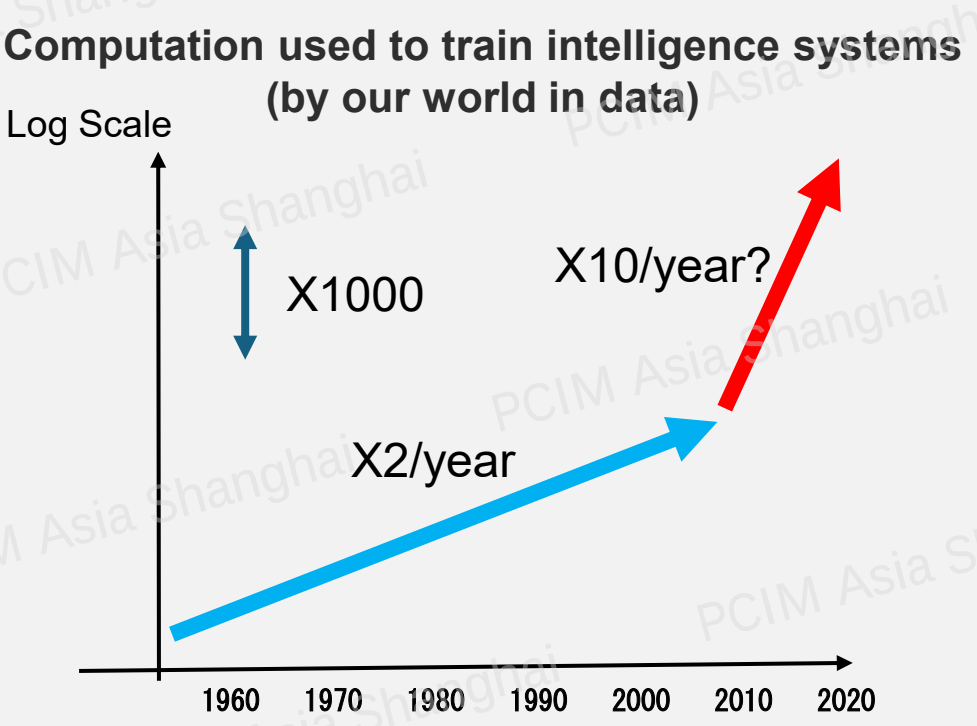
EMIB(Embedded Multi-die Interconnect Bridge

Multiple Small Chips (Tiles) with Different Nodes/Functions are Heterogeneously Integrated ➔ Cost Reduction and System Flexibility

多个具有不同节点/功能的小芯片（瓷砖）异构集成 ➔ 成本降低和系统灵活性

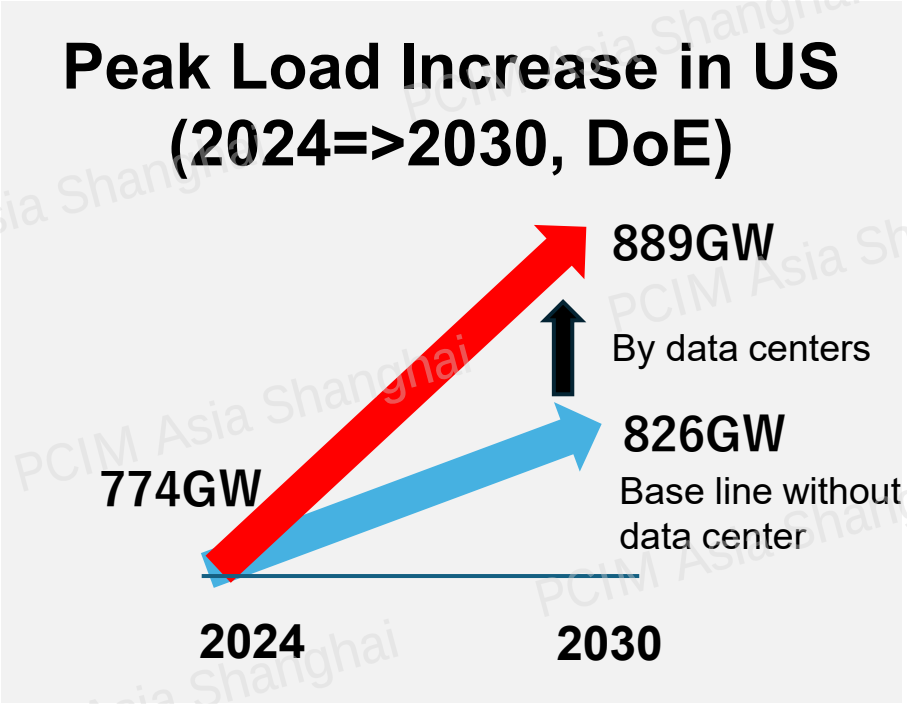
https://www.techpowerup.com/gpu-specs/intel-ponte-vecchio.g1046

AI = Computation and Energy Infrastructure



Data from:
https://ourworldindata.org/grapher/artificial-intelligence-training-computation

https://www.ark-invest.com/articles/analyst-research/ai-training?ref=blog.paperspace.com



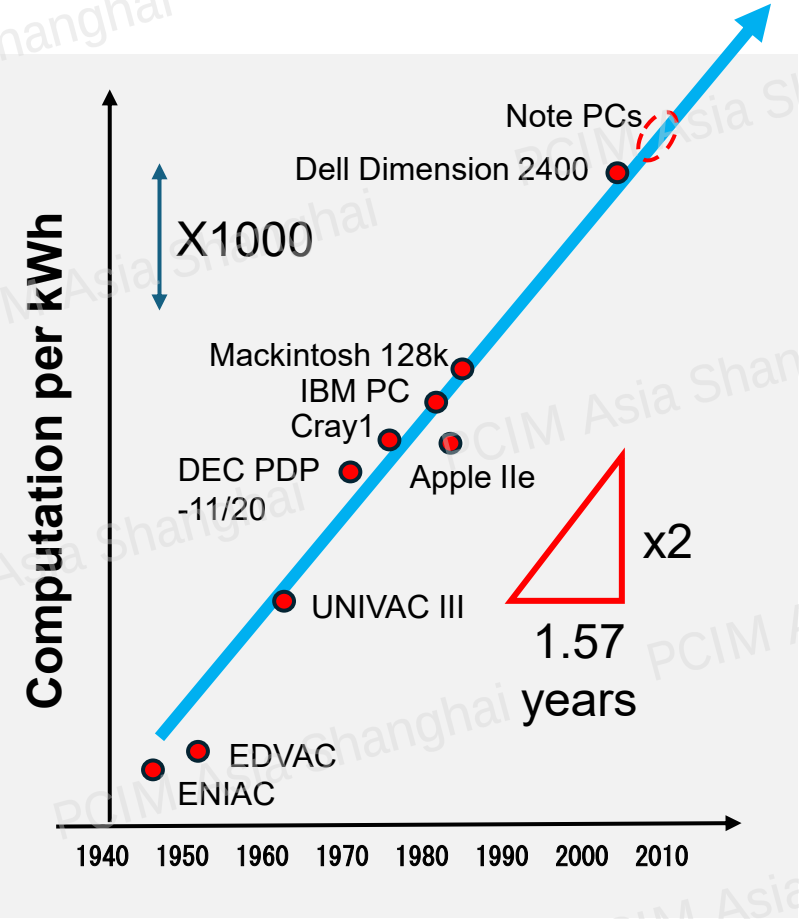
Growth rate of 10GW/Year (only for data center)

Data from DoE, Resource Adequacy Report
Evaluating the Reliability and Security of the United States Electric Grid July 2025

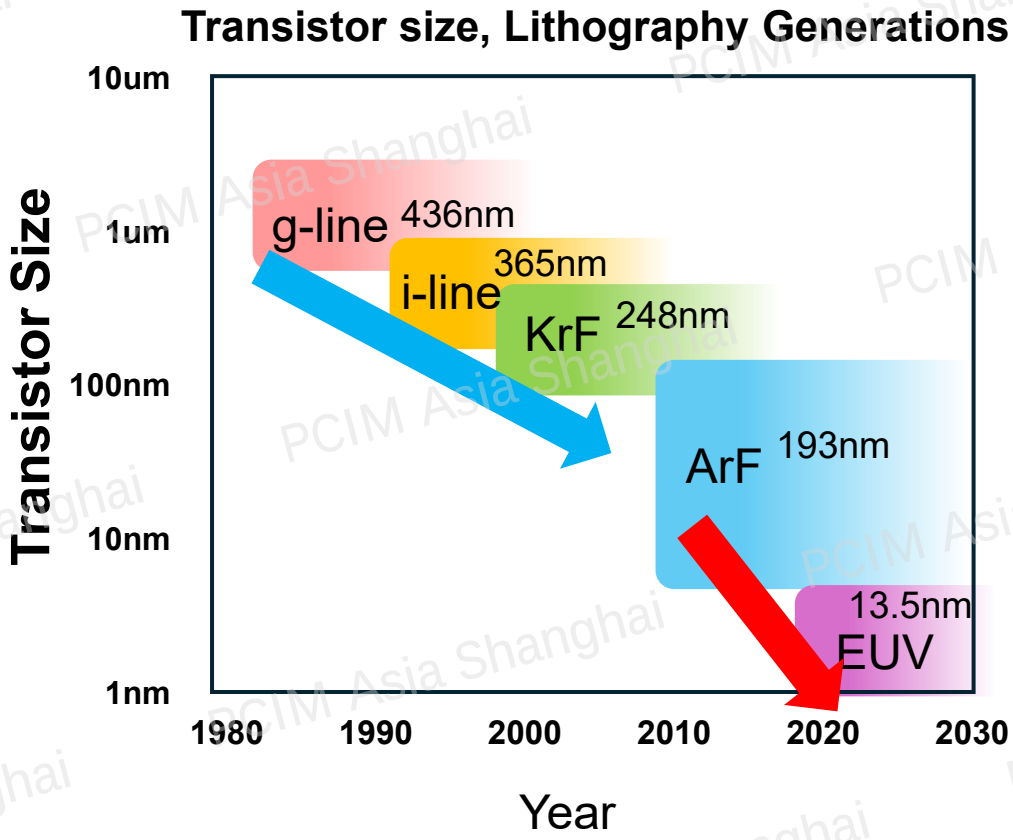
Energy may limit AI Development Speed

能源供应可能限制人工智能的发展速度。

Computation per Energy and Transistor Size



Data from: J. Koomey et al., "Implications of Historical Trends in the Electrical Efficiency of Computing," in *IEEE Annals of the History of Computing*, vol. 33, no. 3, pp. 46-54, March 2011

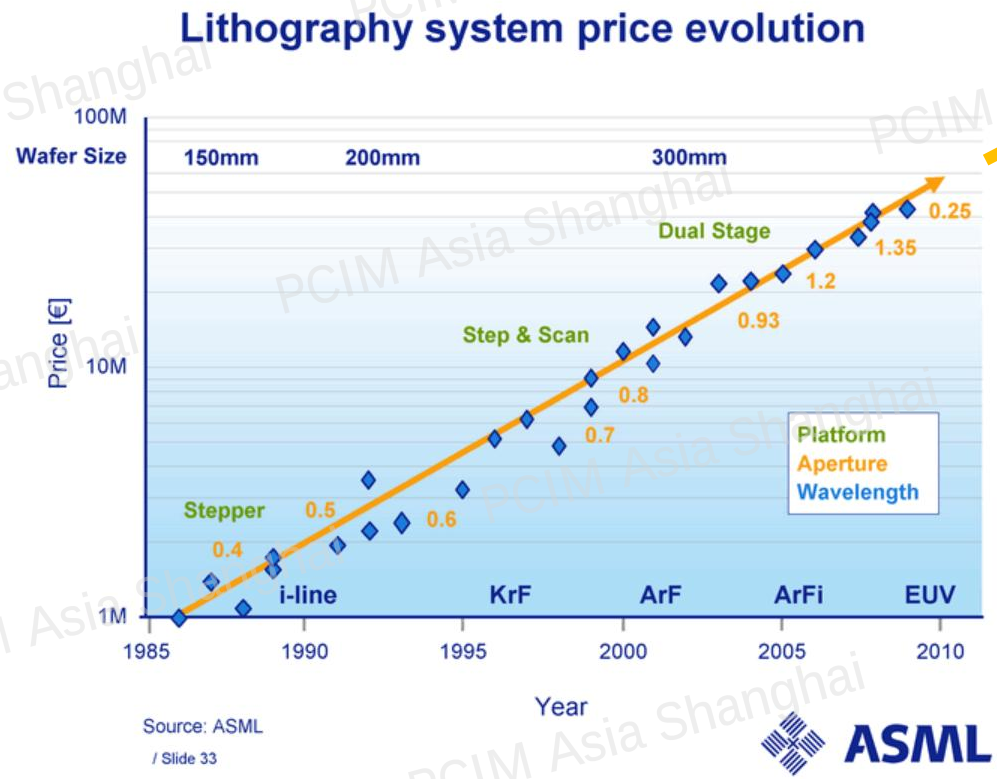


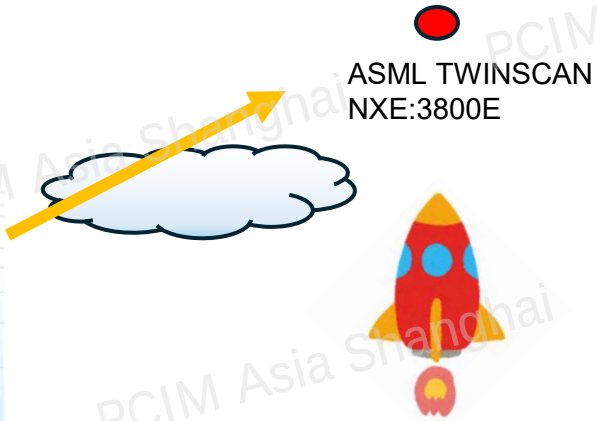
Data from
https://www.tel.co.jp/museum/magazine/report/202310_01/

Minimizing of Transistor Size is the Solution

缩小晶体管尺寸是解决方案

ASML Lithography System Price





ASML光刻机非常昂贵

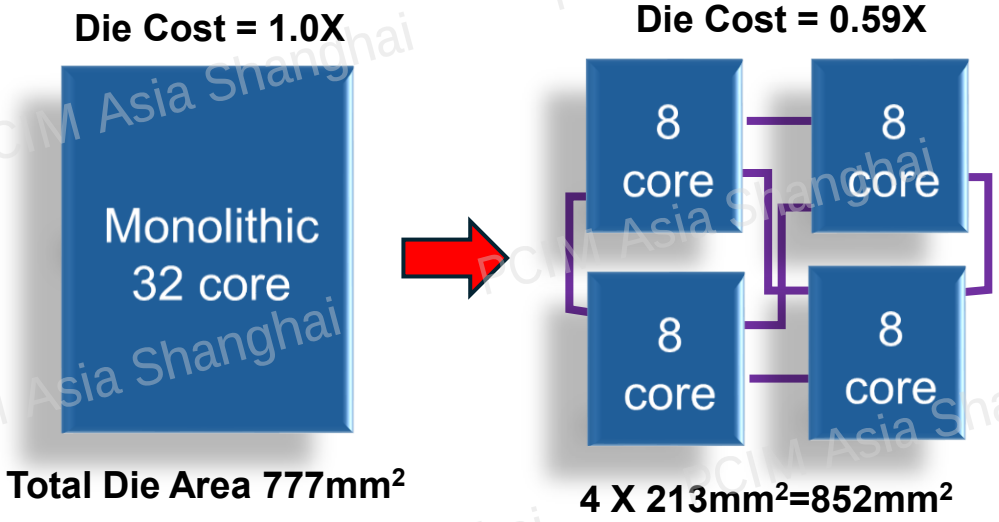
https://www.sec.gov/Archives/edgar/data/937966/000115697308000602/u55770exv99w2.htm

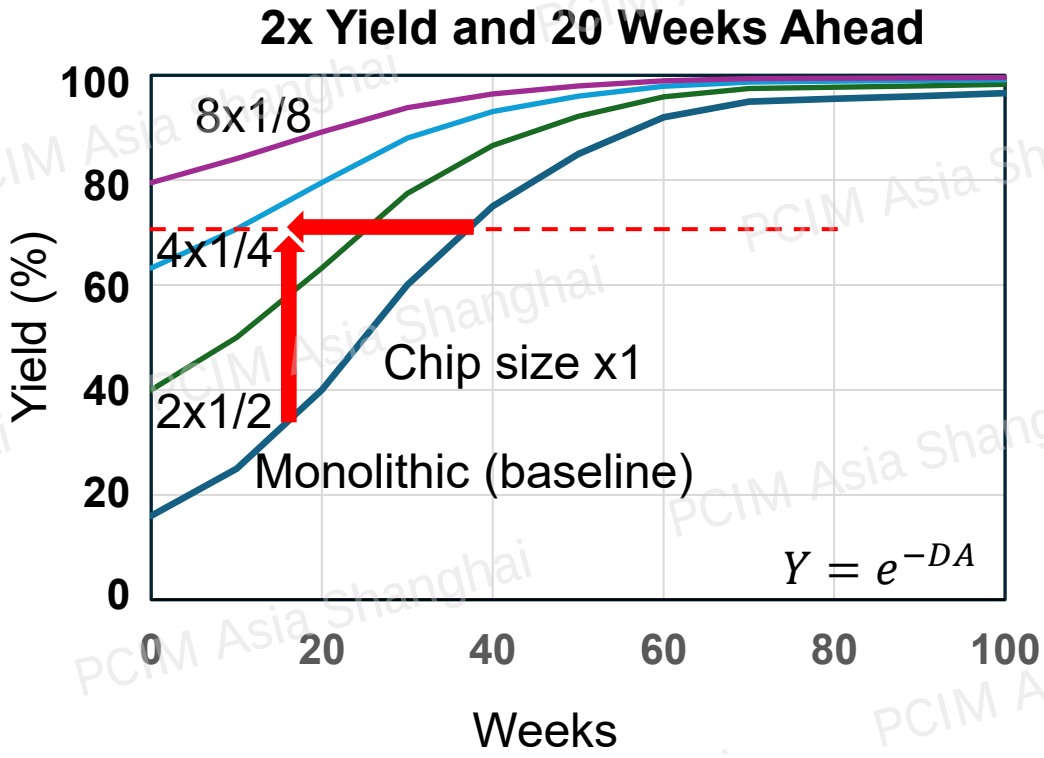
2025

Increasing Chip Costs and Decreasing Yield

芯片成本上升，良率下降

"Chiplet", Smaller Chip Concept





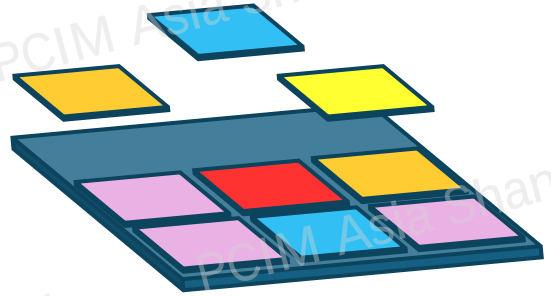
Deta from: L. T. Su et al., "Multi-chip technologies to unleash computing performance gains over the next decade, IEDM 2017, doi: 10.1109/IEDM.2017.8268306.

Chiplet Technology Reduces the Cost and Shorten the Development Cycle

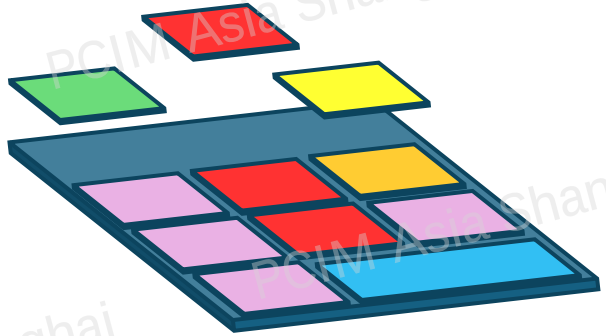
"芯粒"技术可降低成本并缩短开发周期

Chiplet Technology Overview

1. A chiplet is a technology that integrates **small chips** into a package to build **large-scale systems**.



2. It enables heterogeneous integration of circuits and functions across **different process nodes**, while offering high **design flexibility** in system architecture.

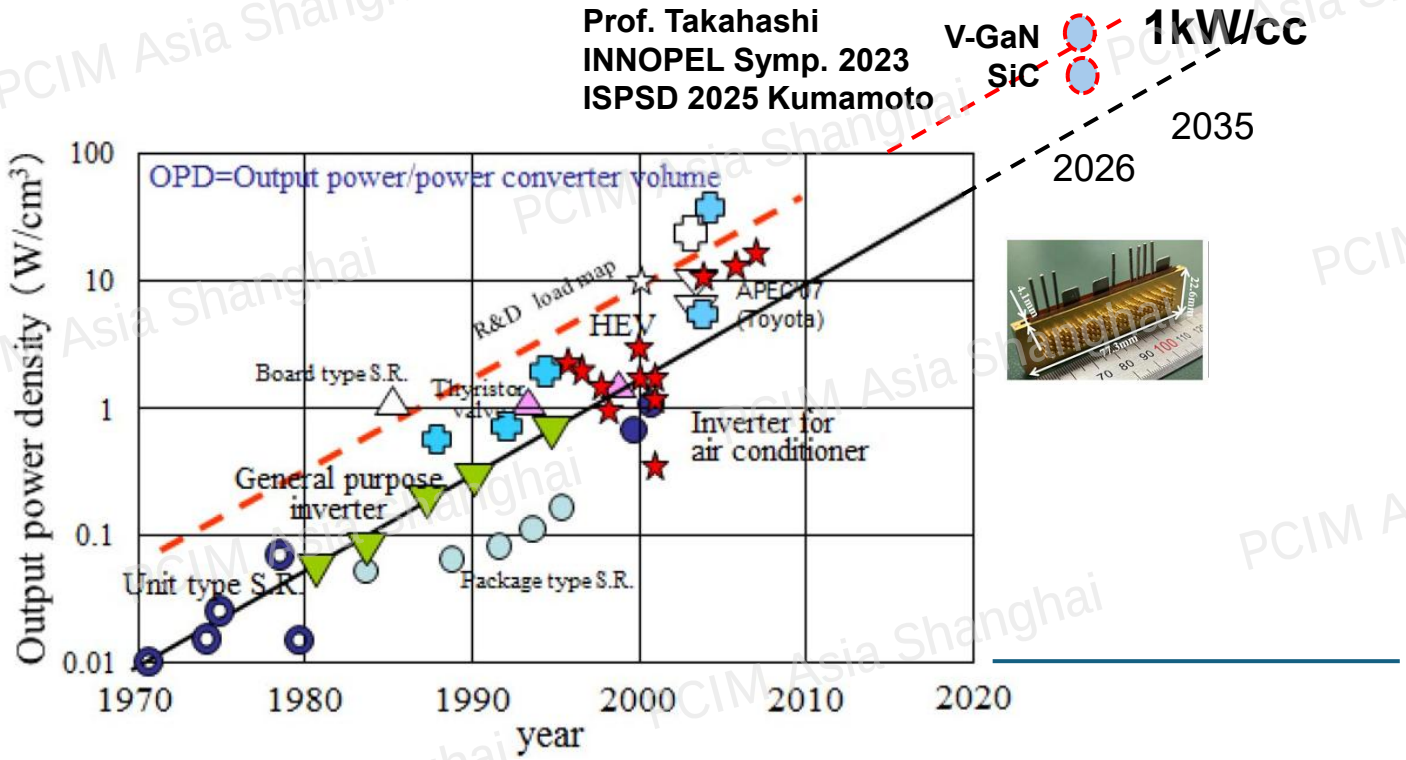


3. Applying chiplet technology may allow the **growth of computation per kWh** for future AI technology with **lower cost.**

Agenda

- "Chiplet" for High Performance Computing
- **Road Maps of Power Semiconductors**
- Why “PowerChiplet”?
  - Chip level
  - Gate drive / Circuit level
  - System level
- Summary

Power Electronics Power Density Trend toward 2035



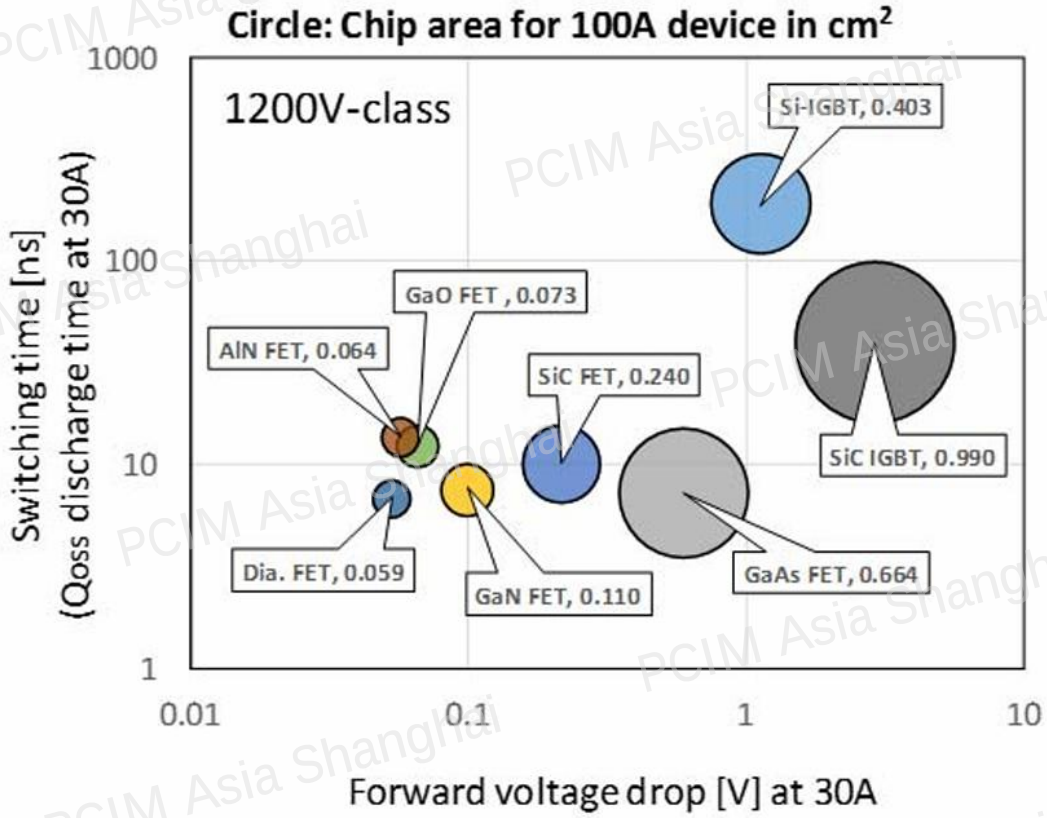
H. Ohashi, I. Omura, Role of Simulation Technology for the Progress in Power Devices and Their Applications, IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL.60, NO.2, 2013

Power Density Increase 10x for Every 15 Years→1kW/cc in 2035

预计功率密度每15年增长10倍，到2035年将达到1 kW/cm³。

WBG Power Semiconductors

Vertical Device



T. P. Chow, I. Omura, M. Higashiwaki, H. Kawarada and V. Pala, "Smart Power Devices and ICs Using GaAs and Wide and Extreme Bandgap Semiconductors," in IEEE Transactions on Electron Devices, vol. 64, no. 3, pp. 856-873, March 2017

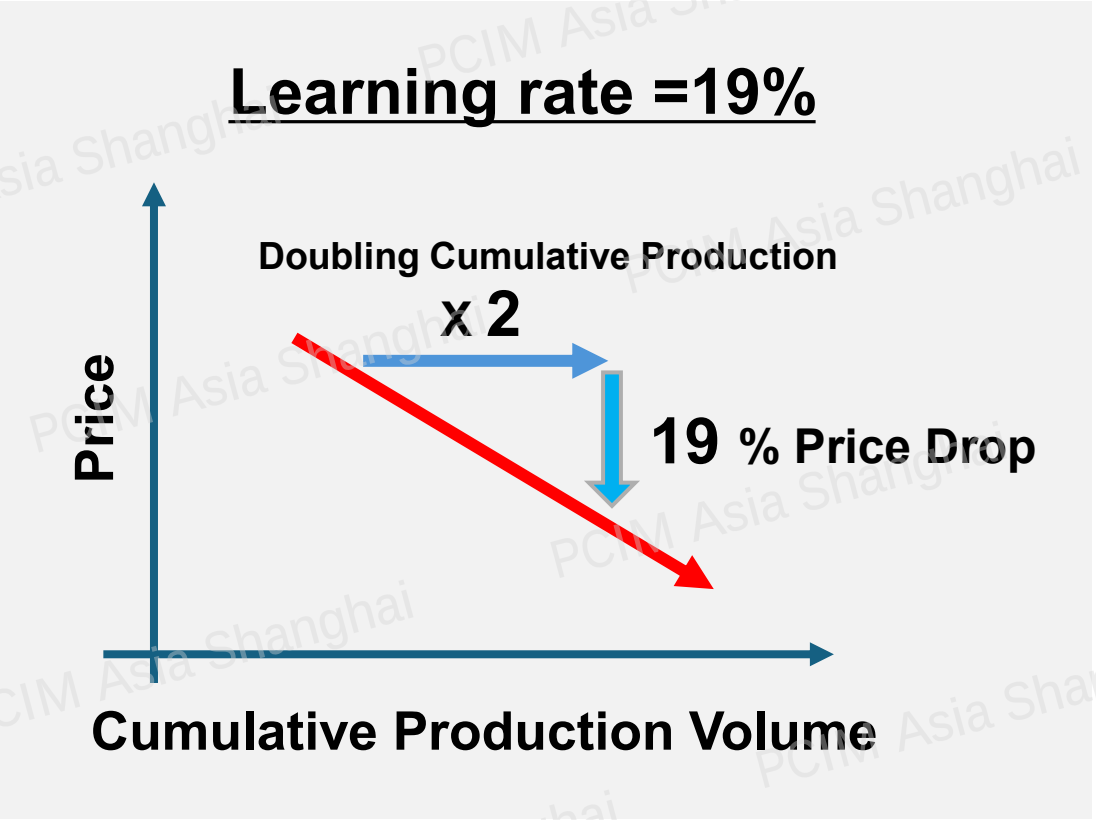
Higher Switching Speed and Lower Conduction Loss with Smaller Chip Size

但开关速度更快，导通损耗更低，芯片尺寸更小 。

Power Electronics Price Trends

Item	Learning Rate	Source
PV module	20%	Bloomberg New Energy Finance
Onshore wind	19%	
Li-ion Battery	19%	Hannah Ritchie, Our world in data, 2021
PV inverter	7%→19%	Agora report, Fraunhofer ISE, Current and Future Cost of Photovoltaics, 2015,
DRAM/Flash	35%	Walden Rhines, Predicting Semiconductor Business Trends After Moore's Law, 2019
Remaining Semis	23%	

Ichiro Omura,
Power Electronics for a Future Sustainable Society,
Keynote at PCIM2022 Nurnberg, May 11, 2022

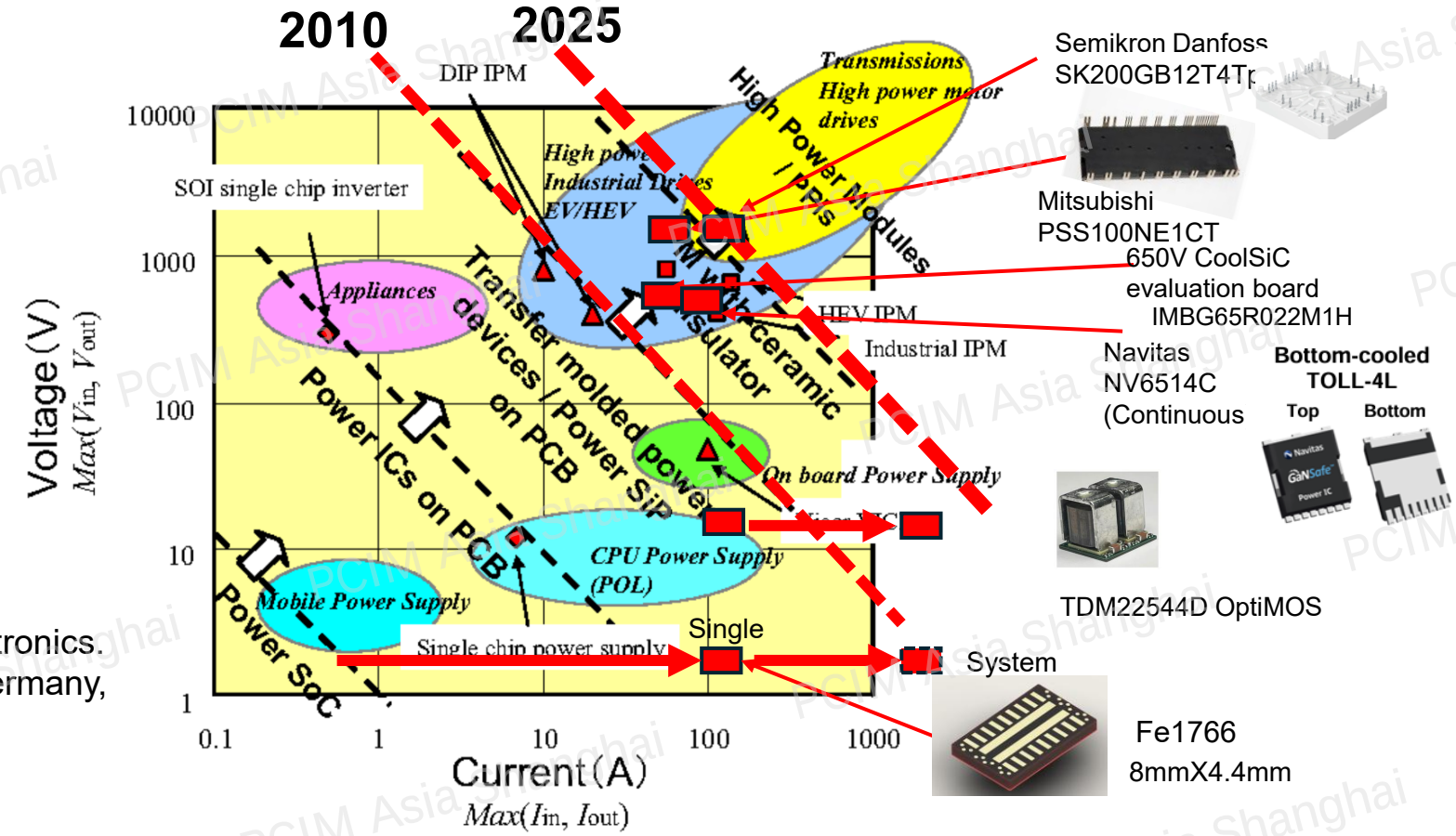


Rapid Price Reduction for Production Volume Increase

生产量增加导致价格迅速下降

Power on/in PCB

10x for 15 years



Ichiro Omura,
Future Role of Power Electronics.
CIPS 2010, Nuremberg/Germany,
Paper 14.2

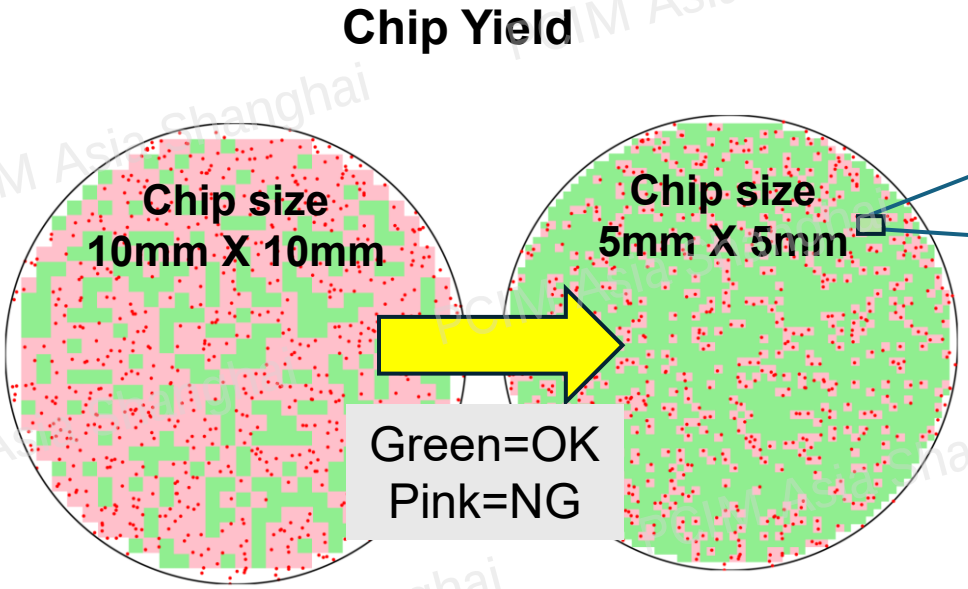
PCB Technology is the Key to Reduce the Costs and Size

PCB技术是降低成本和尺寸的关键

Agenda

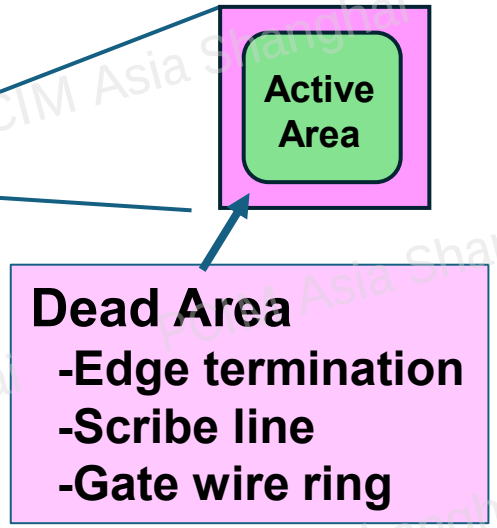
- "Chiplet" for High Performance Computing
- Road Maps of Power Semiconductors
- **Why “PowerChiplet”?**
  - Chip level
  - Gate drive / Circuit level
  - System level
- Summary

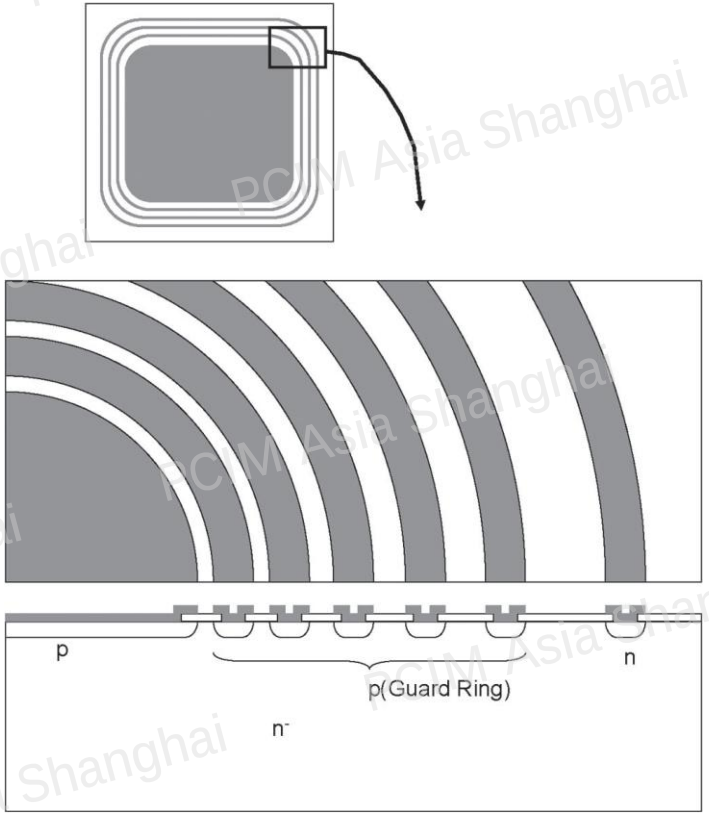
"Active Area" Yield



$$Y = e^{-DA}$$

New Technology and Material
Starts from High Defect Density

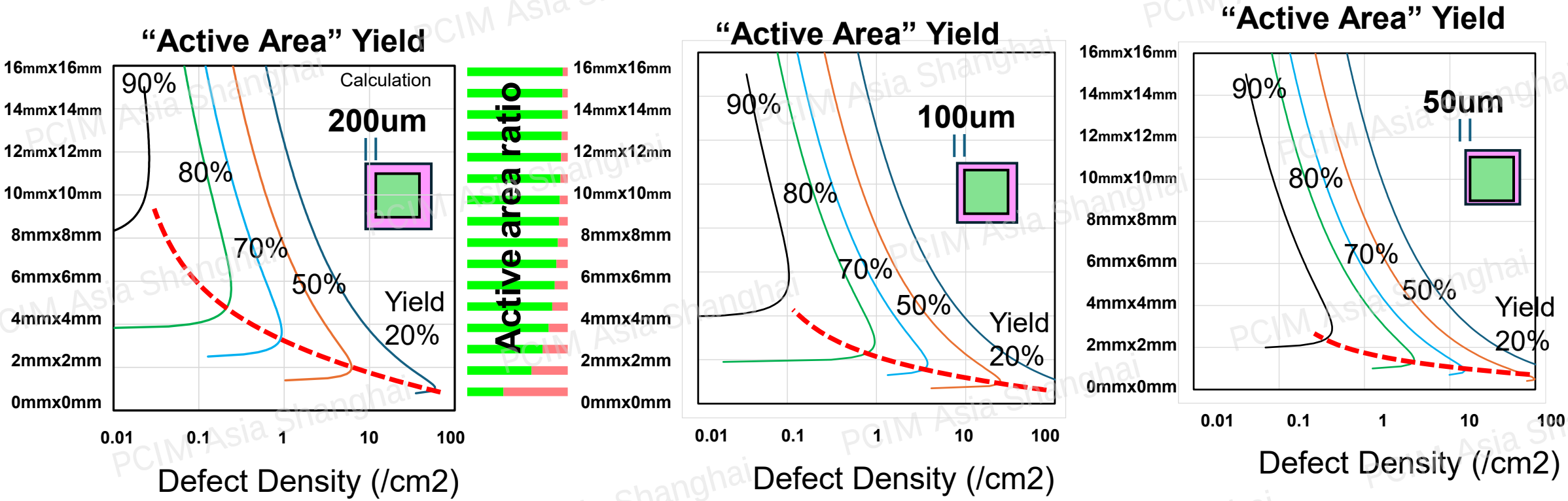




Area Ratio of Total Produced Active Area

总生产活性面积的面积比

“Active Area” Yield for Dead Area on Chip

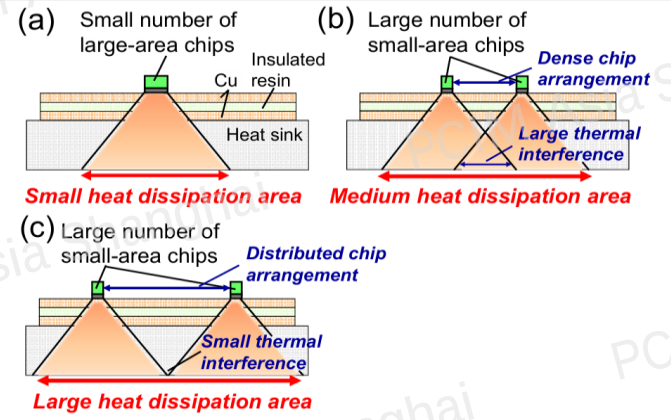


For WBG (High Ecrit), Small Chip Size are Optimum

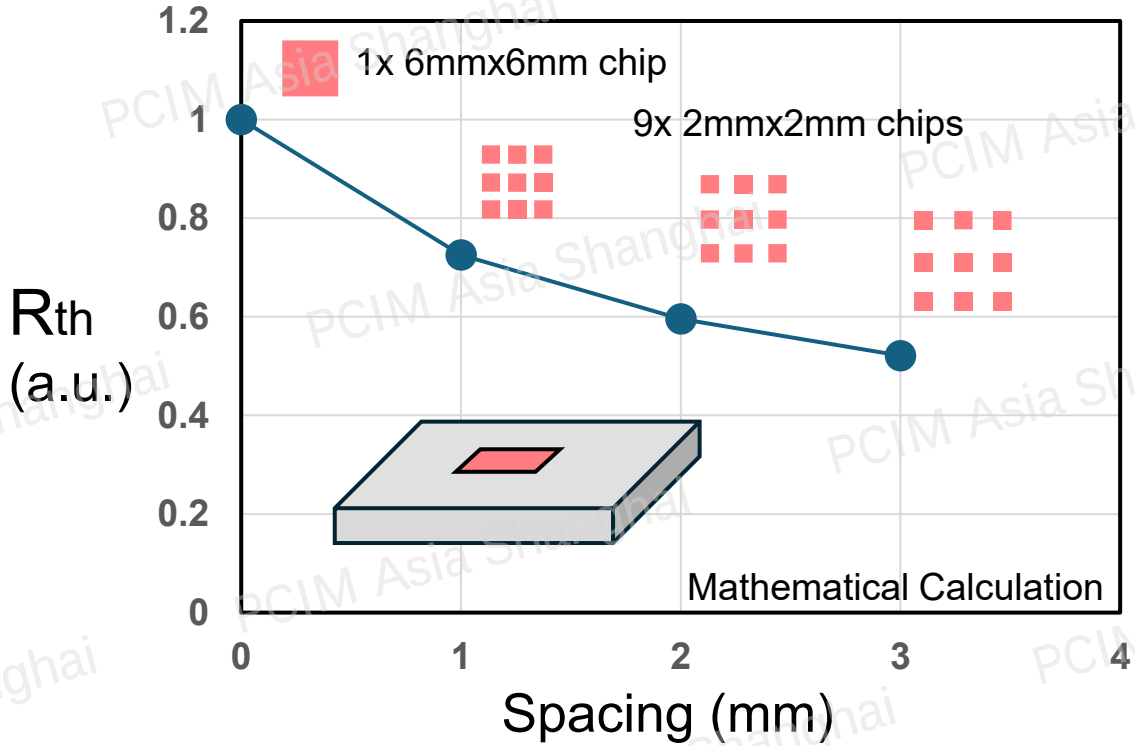
对于WBG（高Ecrit），小芯片尺寸是最佳选择

Multiple Small Chip Layout for Better Cooling

Toshiba, ISPSD2025



Thermal Resistance for Spacing



Small Chip Layout Reduce R_{th} by Half

分布式小型芯片布局将Rth减半

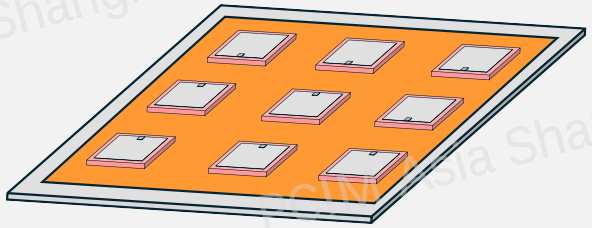
T. Ohashi et al. 37th International Symposium on Power Semiconductor Devices and ICs (ISPSD), Kumamoto, Japan, 2025

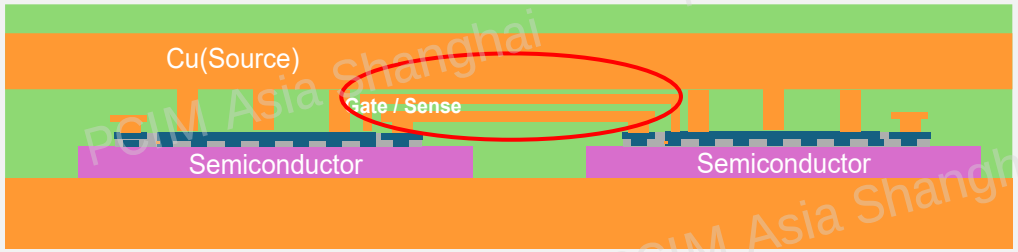
Agenda

- "Chiplet" for High Performance Computing
- Road Maps of Power Semiconductors
- Why “PowerChiplet”?
  - Chip level advantage
  - **Gate drive / Circuit level**
  - System level advantage
- Summary

Low Inductance Wiring for Stable Switching

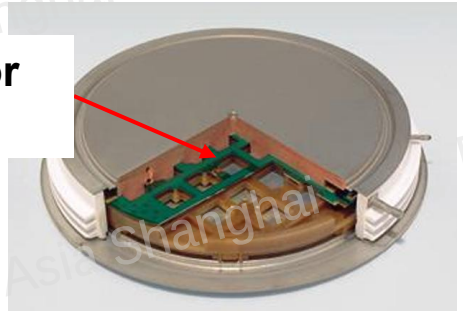
DBC? Cu-Frames? Bonding wires?

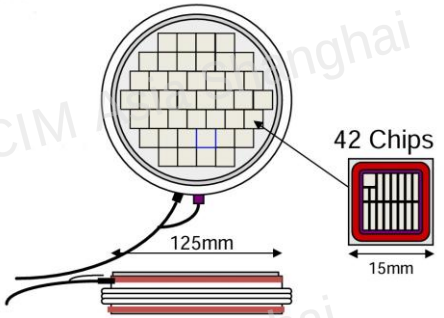




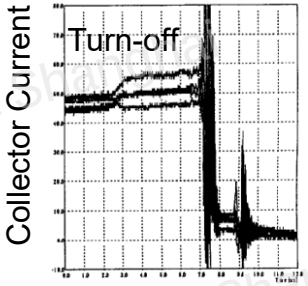
Toshiba PPI (IEGT) 42 Chips Parallel

Low Ls PCB for gate wiring

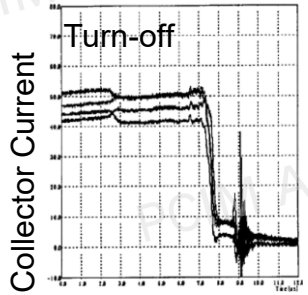




Not Optimized Gate Wiring



Optimized Gate Wiring



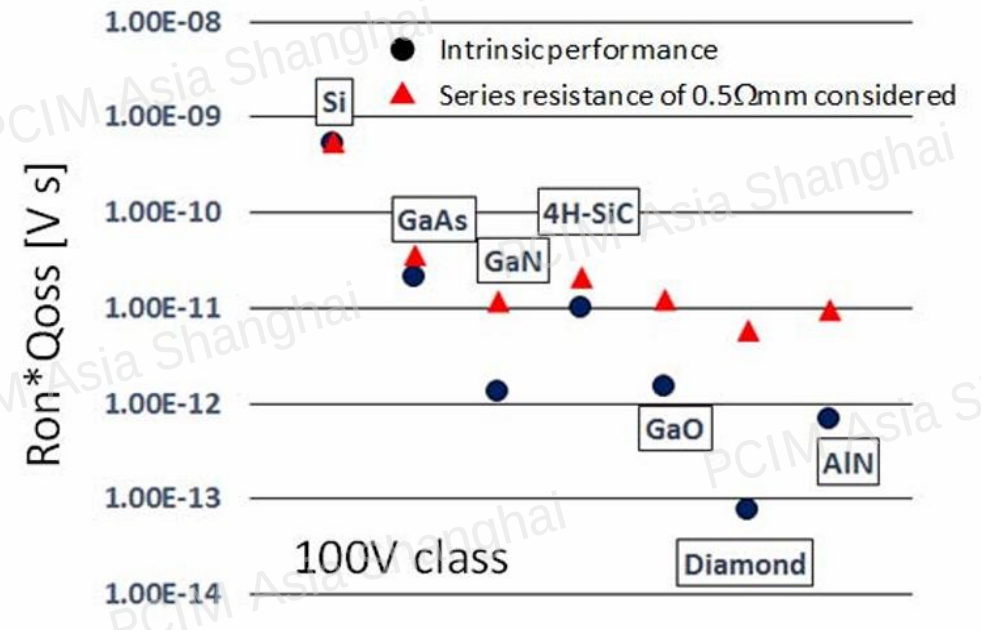
I. Omura et al. ISPSD 2003

Sophisticated Design of Wiring in PCB Enhance Switching Performance

PCB 布线设计精良，提升开关性能

Issue of Parasitic Inductance for High-Speed Switching

Ultra High-Speed Lateral Devices



GaN Transistor	Supplier	di/dt	VDC	Remarks
GS66516T	GaN Sys.	18A/ns	400V	S. Satpahy, Simul. 2021
EPC1010	EPC	9A/ns	100V	M, Danilovic, 2018
EPC2015C	EPC	15A/ns	20V	K. Wang, 2011

T. P. Chow et al., in IEEE Transactions on Electron Devices, vol. 64, no. 3, pp. 856-873, March 2017

K. Wang et al., IEEE Trans. on PE, 2018, doi: 10.1109/TPEL.2017.2749249.

M. Danilovic et al, ECCE 2011, doi: 10.1109/ECCE.2011.6064128.

S. Satpathy et al., ECCE-Asia), 2021, doi: 10.1109/ECCE-Asia49820.2021.9479426.

Very Low Ls (Self or Mutual) Wiring is Required for Advanced Devices

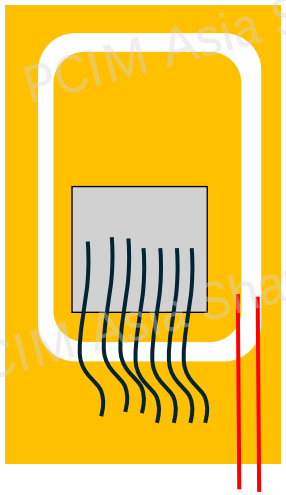
高级设备需要极低的 Ls（自感或互感）接线

Agenda

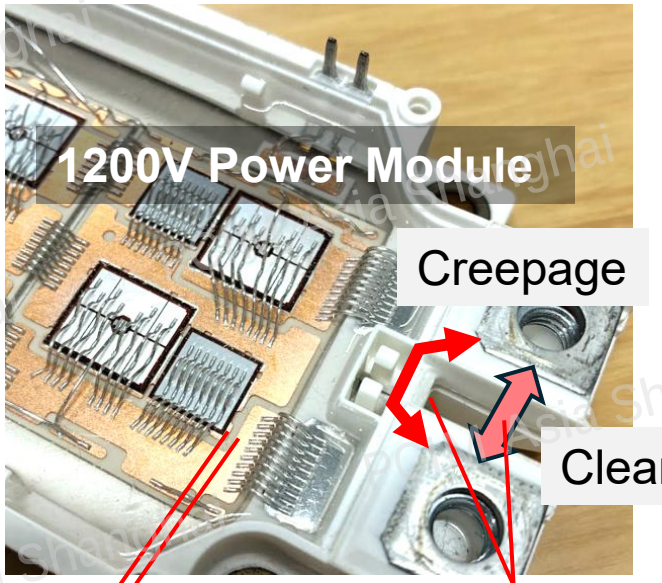
- "Chiplet" for High Performance Computing
- Road Maps of Power Semiconductors
- Why “PowerChiplet”?
  - Chip level
  - Gate drive / Circuit level
  - **System level**
- Summary

Interconnection between Chips and Power Circuit

Clearance and Creepage Distance

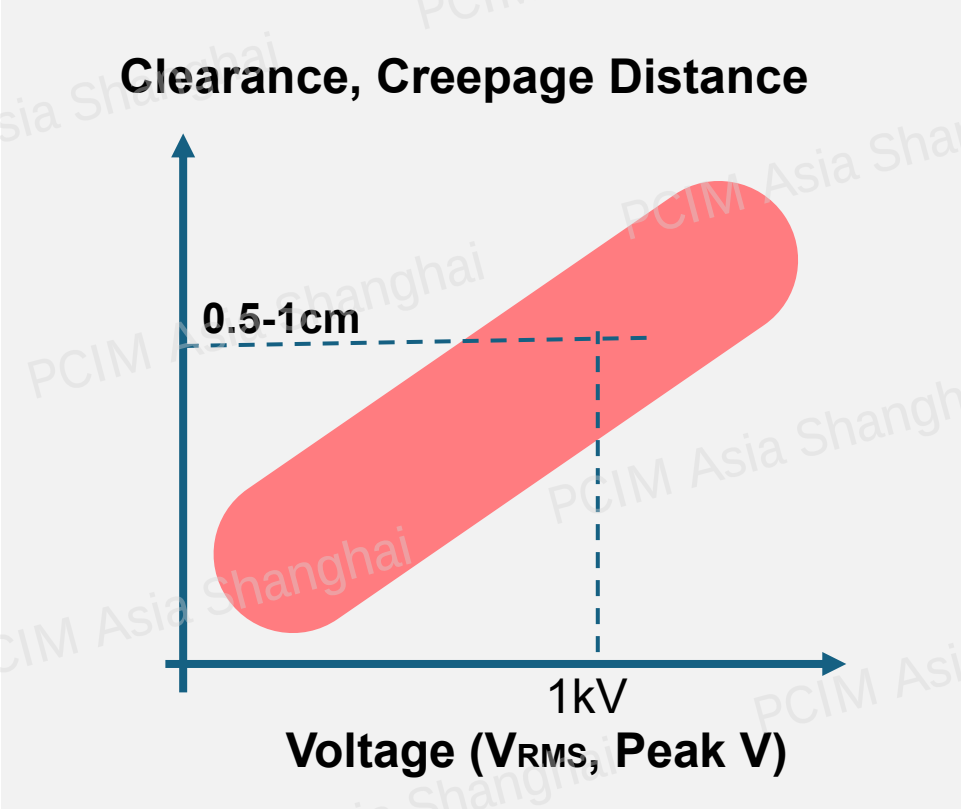


Cu Patten Spacing
Inside Module
~1mm



~1mm

0.5~1.0cm



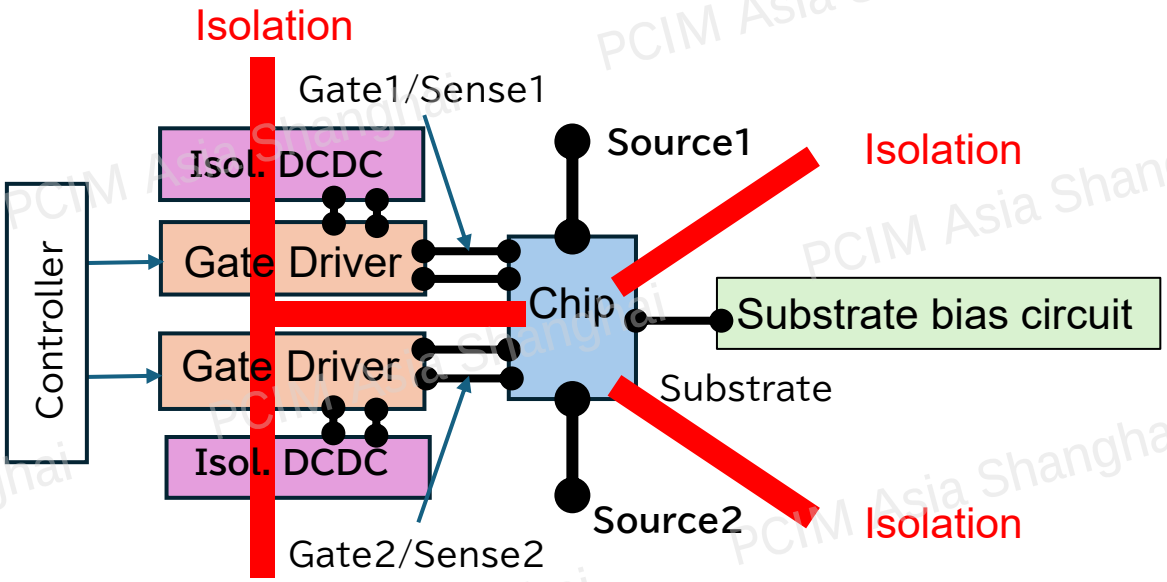
Wiring and Connection INSIDE the PCB to Reduce the Size

封装内部布线和连接以减小尺寸

Needs of System Integration

Complexity of Device Operation

Lateral Bidirectional Device Case



Peripheral Circuits of Chip Need to be Integrated to be the System

芯片外围电路需集成成系统

Chip Embedded PCB
Packaging ➔ System

Level 1: New Packaging of Existing Products **Packaging**
Utilizing existing semiconductor products with updated packaging technologies.

Level 2: PowerChiplets Using Existing Chips **Sub-system**
Combining existing power chips and gate drivers etc. as “Tiles” to enhance modularity and integration.

Level 3: PowerChiplets with Dedicated Chips **Sub-system Plus**
Developing power chips and gate driver etc. specifically designed for PowerChiplet.

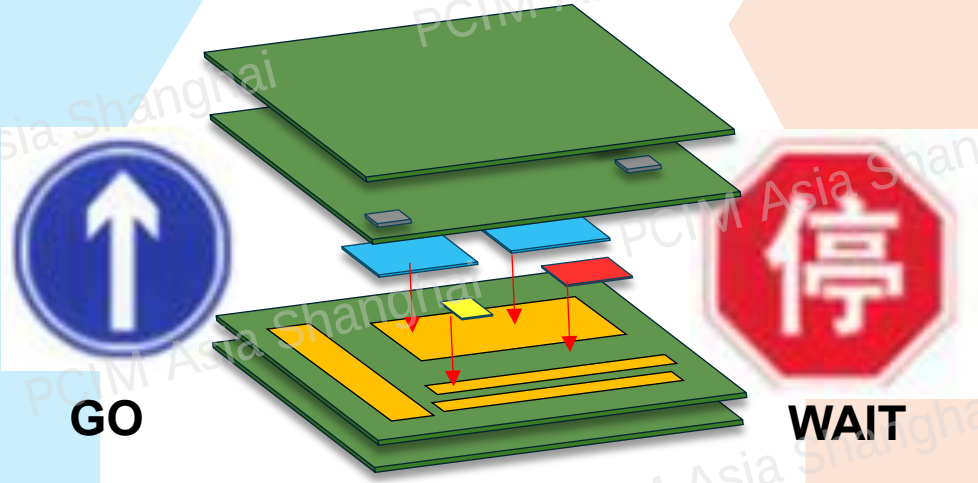
Level 4: System-Level Power Chiplets **System**
Constructing entire power electronics systems using PowerChiplet technology.

Agenda

- "Chiplet" for High Performance Computing
- Road Maps of Power Semiconductors
- Why “PowerChiplet”?
  - Chip level advantage
  - Gate drive level advantage
  - System level advantage
- **Summary**

Why PowerChiplet

- **Chip Level**
  - Chip Cost Reduction
  - Thermal Resistance Reduction
- **Gate Drive / Circuit Level**
  - Stable Switching (No oscillation)
  - High Speed Switching (Reduction of Ls)
  - Solve the Complexity
- **System Level**
  - Size Reduction of Connection to Power Circuit (Creepage, Clearance)
  - PE System Level Cost Down

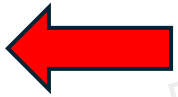


PowerChiplet

- Test
- Co-Design
- Standard (3DBlox?)
- Reliability
- Cost
- Recyclability
- Passive Components
- Isolation (Electrical, Thermal, Signal)
- Others

Presentations

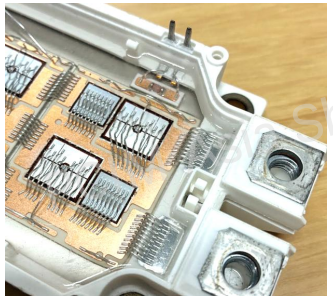
- **Power Chiplet Technology for Next Generation Power Electronics Systems**
  Speaker: Ichiro Omura, Kyushu Institute of Technology, JP
- **Advanced Packages With Power-On-Substrate Solutions**
  Speaker: **Frye Fung**, Zhuhai ACCESS Semiconductor Co., Ltd.. CN
- **Chip Embedded Panel level Power Package for AI and Vehicles**
  Speaker: **Yoshiaki Aizawa**, Aoi Electronics, JP
- **Novel Integration Concepts for Power Electronics - Embedding of SiC MOSFET for High-performance Power Modules**
  Speaker: **Lars Boettcher**, Fraunhofer IZM Berlin, DE
- **Discussion**



Packaging for PowerChiplet

Power Module

Chip
↓
Solder on DBC
↓
Solder on Base Plate
↓
Housing + Silicone filler + Lead frame
↓
PCB for gate wiring, Controlling
↓
Assembling to heat sink
↓
Wire Frame connection

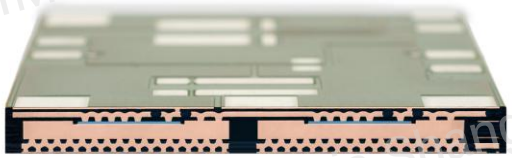


Transfer Mold Module

Chip
↓
Solder on Lead Frame
↓
Molding
↓
Assembling to PCB
↓
Heat sink

Chip Embedded PCB

Chip
↓
Assembling in PCB Process with other chips
↓
Heat sink



Schweizer

Infineon