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Chip Embedded Panel level Power Package for AI and Vehicles

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AOI ELECTRONICS CO.,LTD.

FOLP® Technology Direction (Trend)

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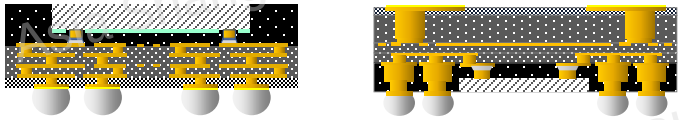
RDL-first *(fine pitch/multi-layer)*

High Frequency

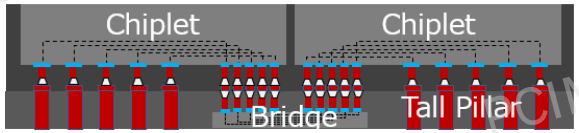
Multi-Layer, 3D FOLP®



High Via connection reliability
Deep plugged Via
Low RF signal loss
(Low Df material)

High-end Logic

Fine pitch FOLP® Chiplet



Fine pillar pitch
Fine Line/Space
High yield (Simple structure)

Chip-first *(high heat dissipation/low resistance)*

Power Module

Thinner , Heat dissipation FOLP®

Low electrical resistance wiring
Low inductance wiring
High heat dissipation
(High thermal conductive material)
High operation temperature
(High Tg material)

Outline

- ✓ Background
  - Why are Chip Embedded Packages required?
  - Chip Embedded Package Technologies

- ✓ Chip Embedded Power Package for AI/Date center applications
  - Coreless Chip Embedded Technology (AOI Panel Level Package)
    - Ex. Thin Multi chip voltage regulator (and with built-in inductor)

- ✓ Chip Embedded Power Package for Automotive applications- Power Sub Module
  - Packaging Technologies
  - AOI Panel Level Power Chip Embedded Technology
    - Ex. Chip embedding process with thick Cu RDL
      - Cu direct plating on the back side of power chips

- ✓ Summary

Background

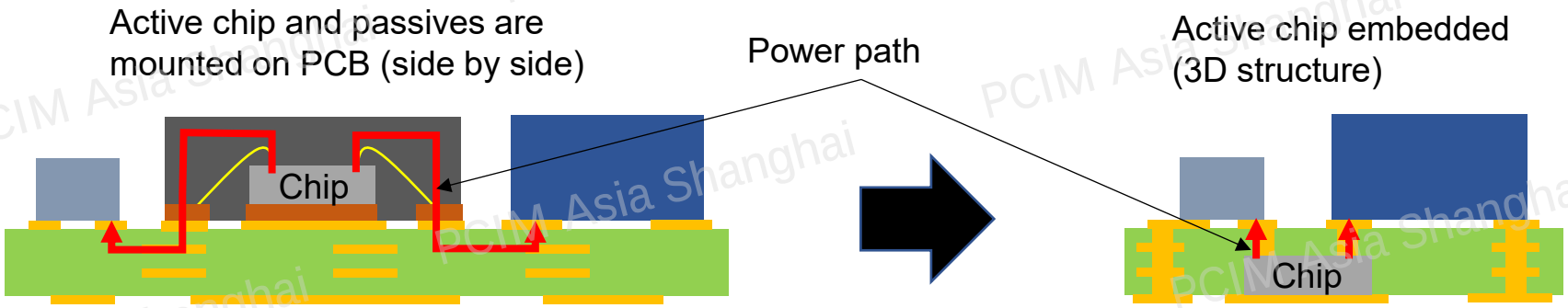
- Power semiconductor plays as a key role in the rapid development of automotive (EV) due to environmental issues
- AI/data center require high efficiency power supply system due to increasing power consumption
- As power supply output current increasing, wiring resistance is a big issue about power distribution loss.
- Reducing parasitic inductance, wiring resistance, and shortening the current loop are necessary in high density environment.
- Chip-embedded packages (PoP/CoP/3D-SiP) can shrink size and increase current density.
- Inverters and DC/DC converters are the need for efficient power management system.

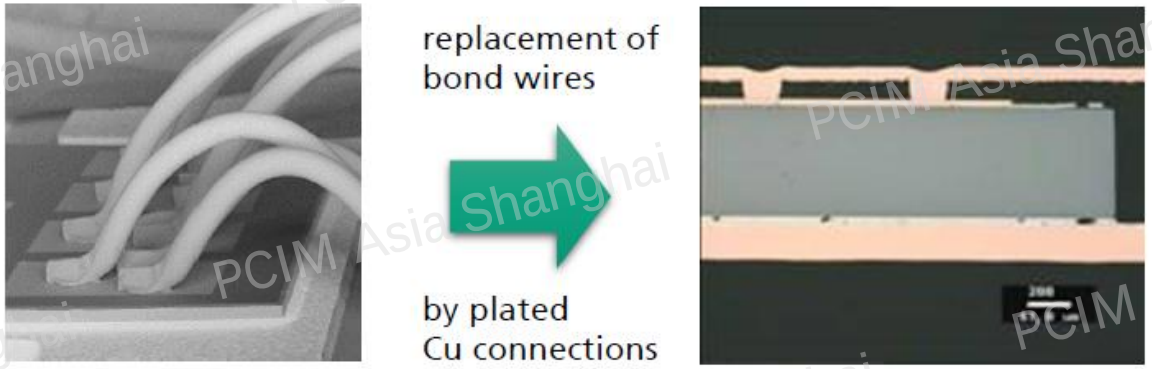
Source : NTT Corporation

Source : TOYOTA corporation

Why are Chip Embedded Packages required?

- Benefits of Chip Embedding Packaging





Motivation

Smaller and Thinner package
Lower resistance
Lower inductance

Source : NEPCON Japan 2025 Fraunhofer IZM

Chip Embedded Package Technologies

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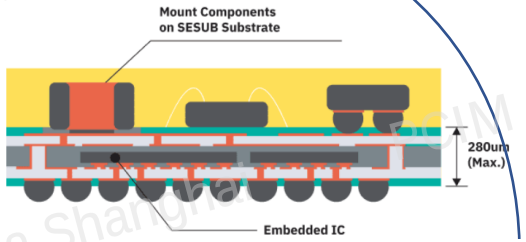
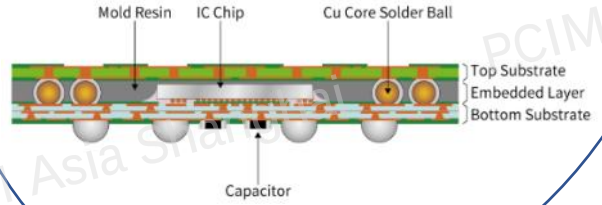
SESUB



Source : ASE

MCeP



Source : SHINKO Corporation

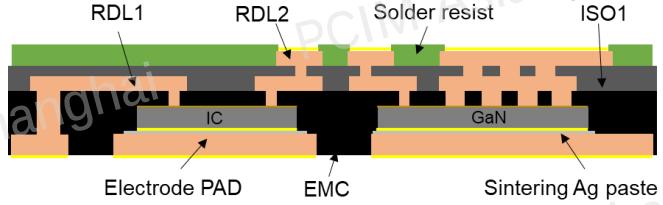
PCB Substrate base

Panel base (Panel level package)

Power core Module Package

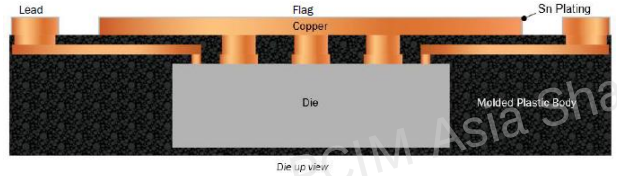
Source : IMAPS Advanced Packaging for Power Electronics 2024 AOI

Thinner Power Module Package



Source : IMAPS DPC 2023 AOI

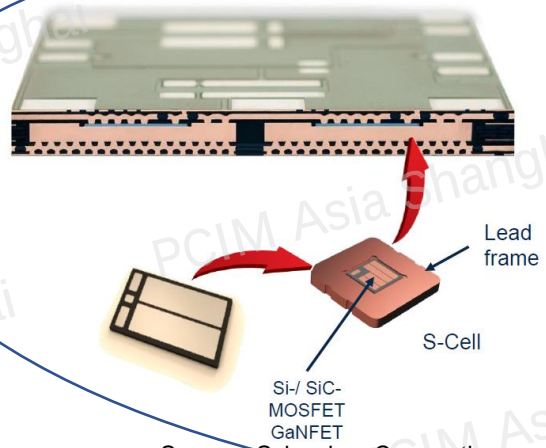
MDQFN



Source : DECA

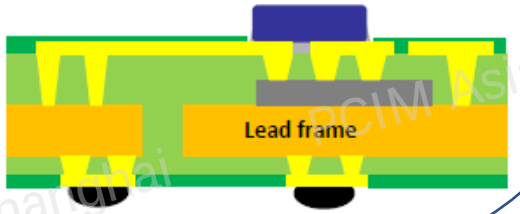
Lead frame base

P2 Pack



Source : Schweizer Corporation

aEASI P1



Source : ASE

Chip Embedded Power Package for AI/Data center applications

Source : NTT Corporation

AI / Data center Application

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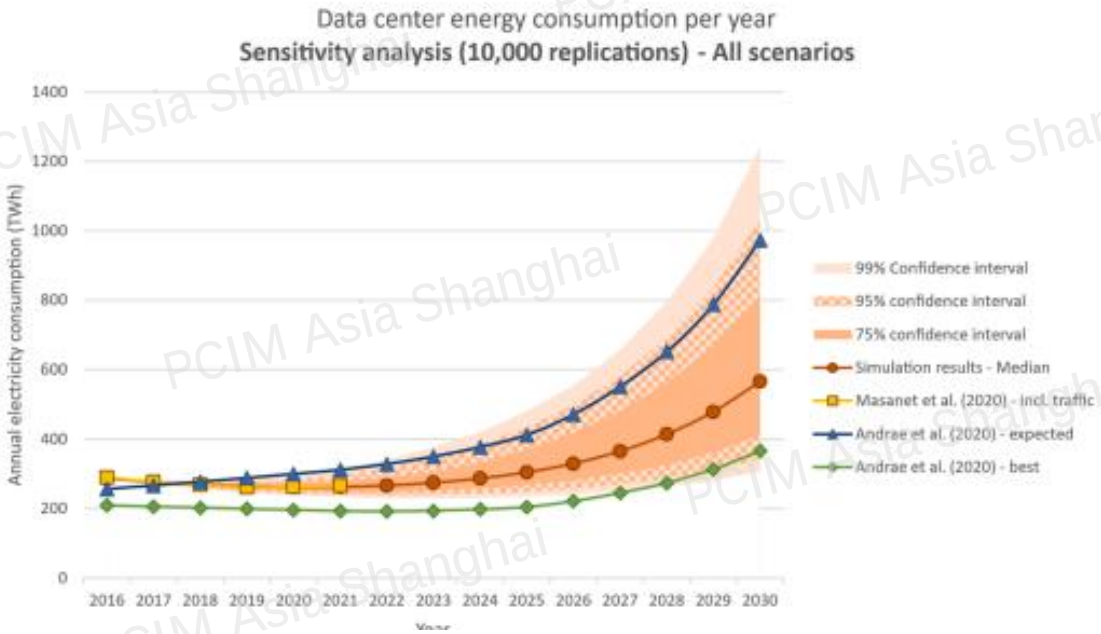
- Applications : Power Supply System

Source : NTT Corporation



Source : University of Twente, the Netherlands

- ✓ AI/Data Center requires high efficiency power supply system at both high voltage and low voltage levels due to increasing power consumption.
- ✓ As power supply output current and switching frequency increase, wiring resistance and inductance are a major concern for power distribution losses and power integrity.
- ✓ Regarding the low voltage stage, placing the voltage regulator (VR) and passives close to the active die (CPU/GPU/HBM, etc.) is very important for power integrity (PI).
- ✓ Substrate embedded VR and passives are a good solution for PI improvement.
- ✓ The embedding of the power module and inductor is a big challenge due to the high profiles.

Power delivery structure of the AI server system

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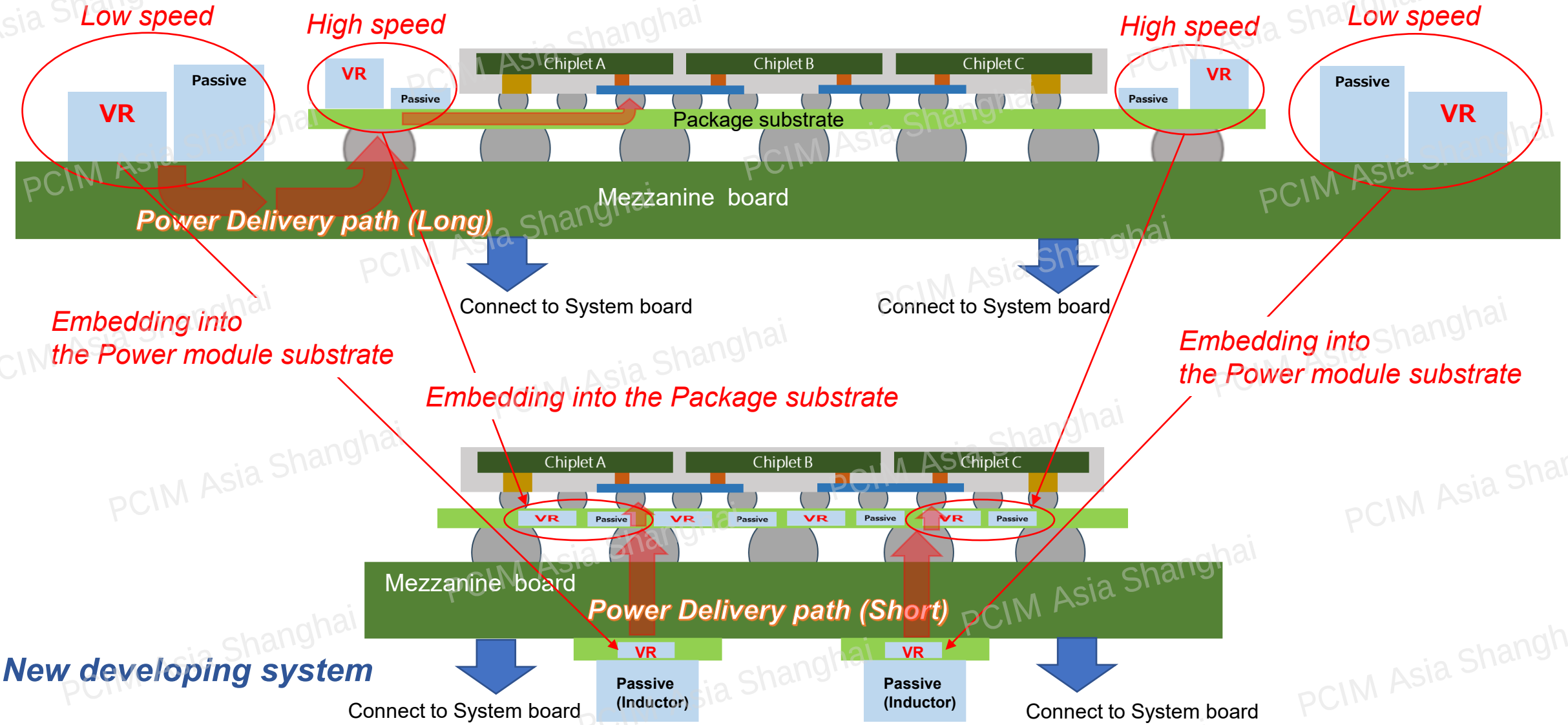
Today's typical system



New developing system

Thermal Resistance Simulation Comparison between Panel Level and PCB Based Package

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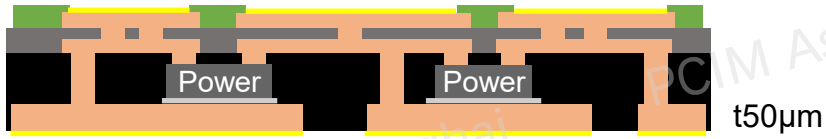
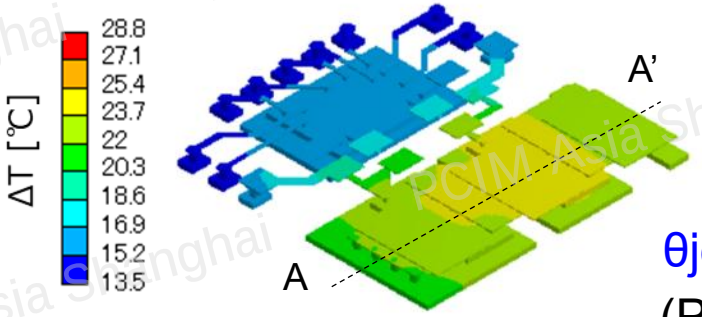
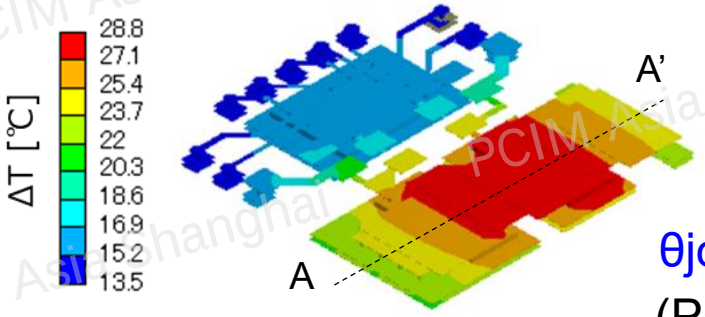
■ Simulation result

	Our Concept package (Panel Level Package)	PCB prepreg package (assumption)
Structure		 Via : φ0.1mm, pitch 0.6mm
Thermal simulation result	Inside the Package image  θjc : 0.5 [°C/W] (Package only) Cross-section A - A' 	Inside the Package image  θjc : 3.7 [°C/W] (Package only) Cross-section A - A' 

The thermal resistance of our concept package is very low, and it has the advantage of quickly dissipating heat to the substrate side.

Coreless Chip Embedded Technology (AOI Panel Level Package)

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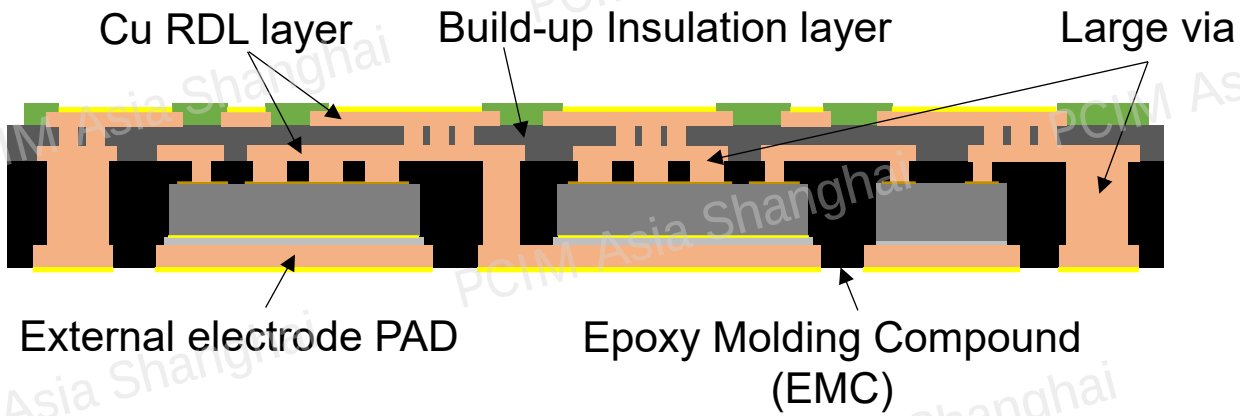
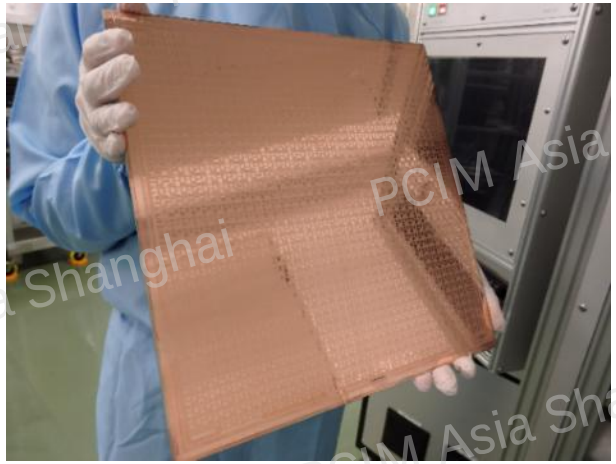
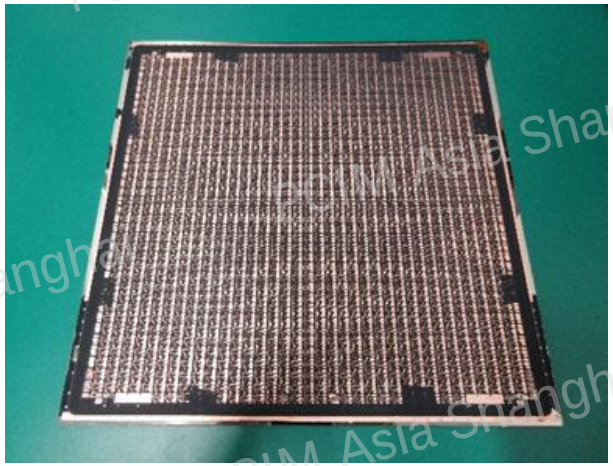
AOI's new approach of ***Ultra thinner, Higher heat dissipation*** chip embedded technology in analog and power solutions.





Features of this concept

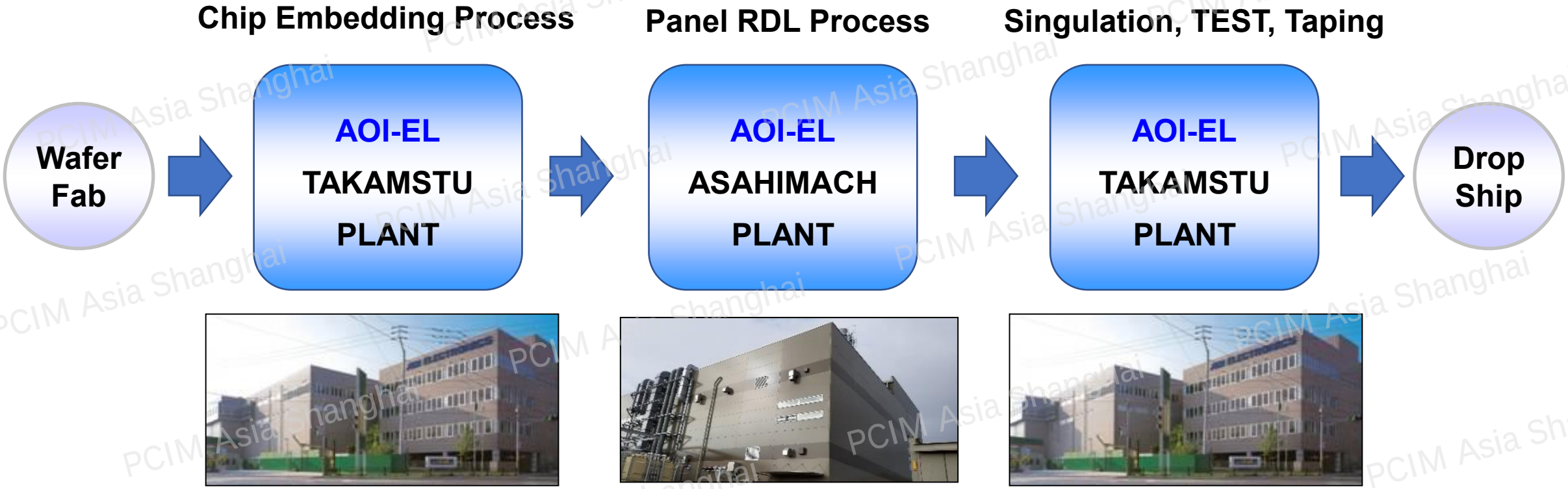
- Unique Coreless structure with all-Cu plating embedding method, using power customized fan-out processes
- Panel form of 300 mm square with cost benefit
- Smaller and Ultra thinner module package with coreless structure
- Excellent thermal property with large electrode pad and large via filling
- High reliability and short TAT with one stop solution (from panel substrates to package assembly in-house)



Source : IMAPS DPC 2023 AOI

Manufacturing Process Flow for a Prototype

- Panel level package manufacturing flow



We can perform one-stop production in-house, from panel substrates to chip embedding process, panel RDL process and package assembly.

Basic Process Flow for a Prototype

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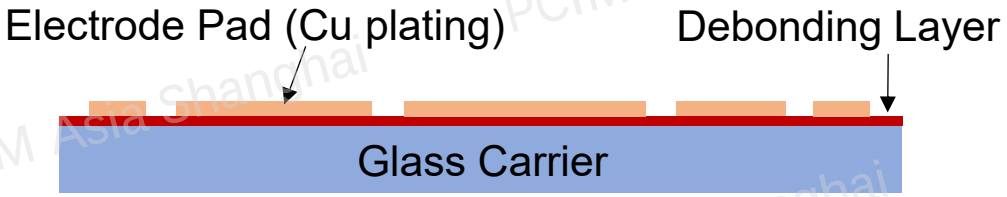
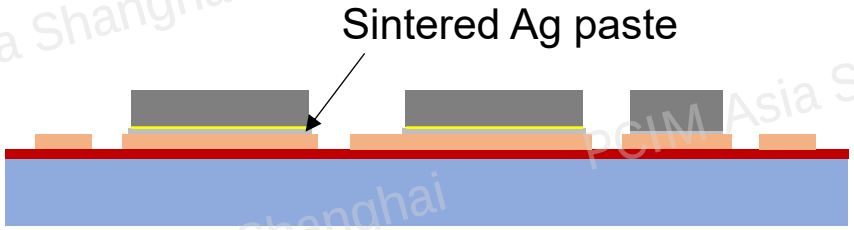
■ Basic Process flow (1)

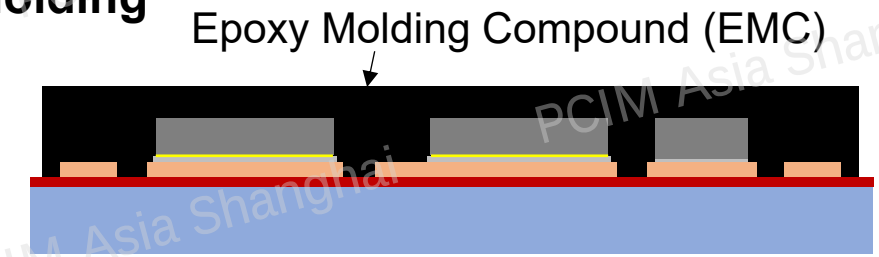
1. Electrode Pads Formation on Glass Carrier



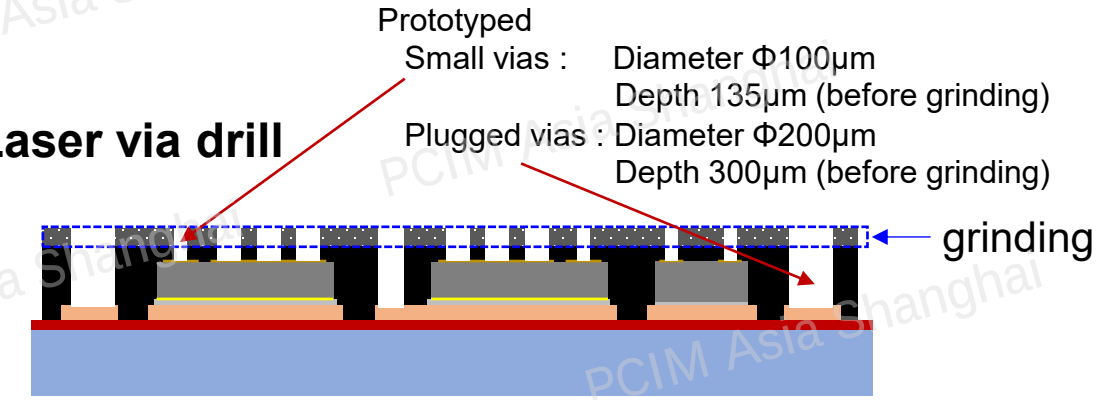
2. Controller and Power Chips Bonding



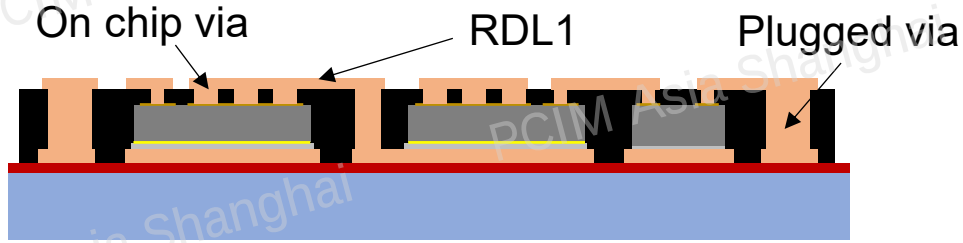
3. Molding



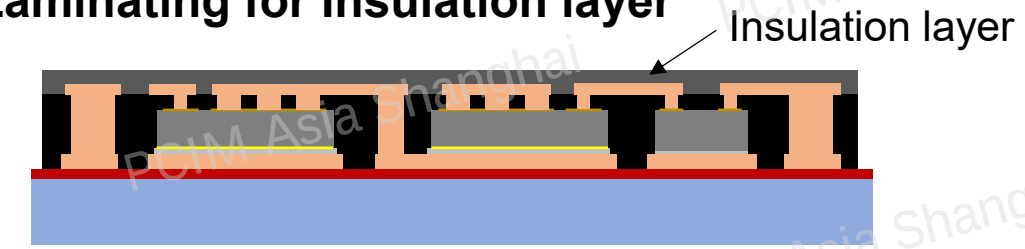
4. Laser via drill



5. Cu plating for Via-filling and RDL1



6. Laminating for Insulation layer



Basic Process Flow for a Prototype

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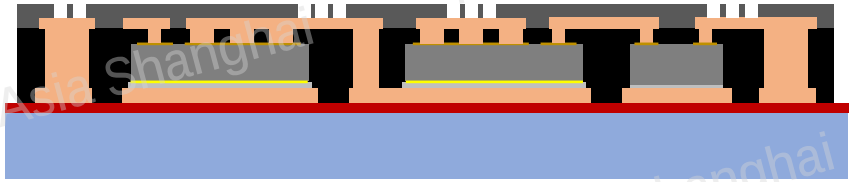
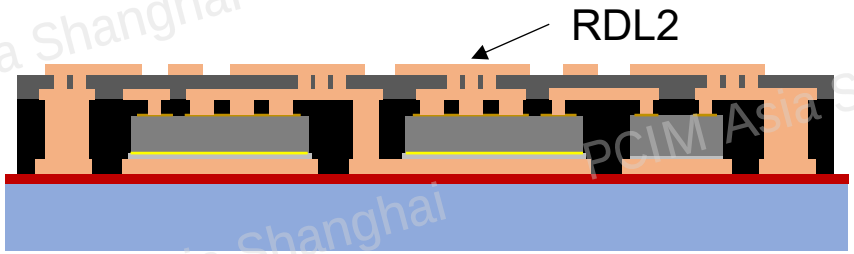
- Process flow (2)

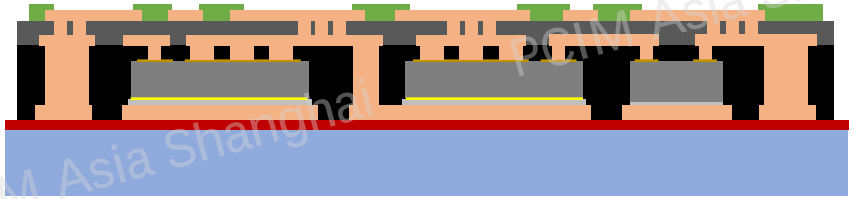
7. Laser via drill



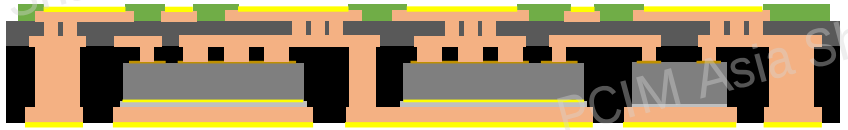
8. Cu plating for Via-filling and RDL2



9. Solder resist formation



10. Glass Carrier Debonding / Terminal plating / Singulation



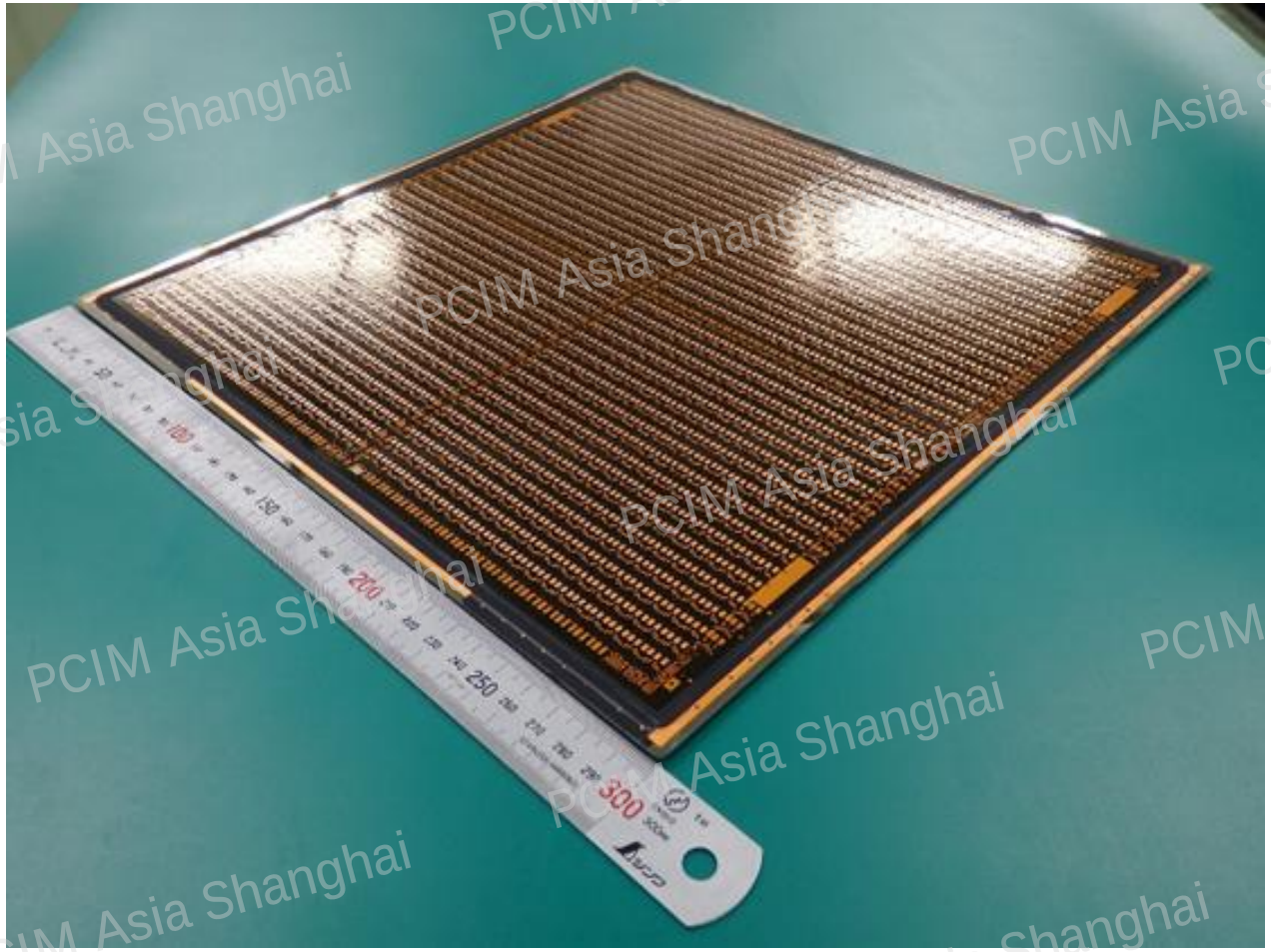
Our usual inspection or test

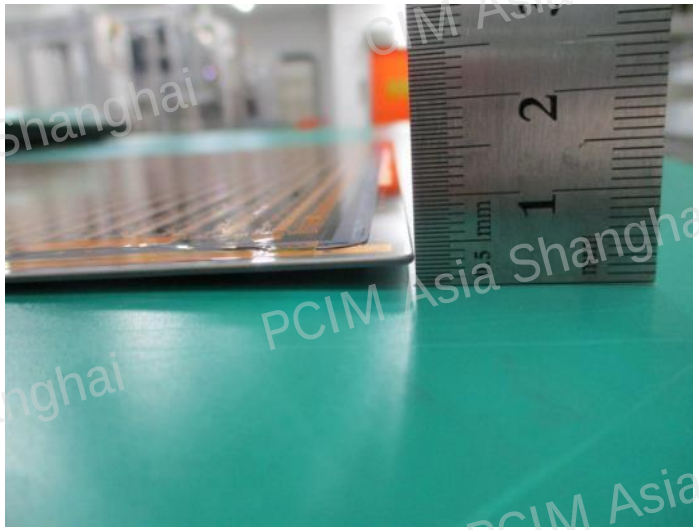
- Pattern inspection for each process
- Open/short test for checking internal connection
- Optional function test

Trial production and evaluations for a Prototype

- 300 mm square Panel-level photo

Warpage Before singulation (with Glass Carrier)

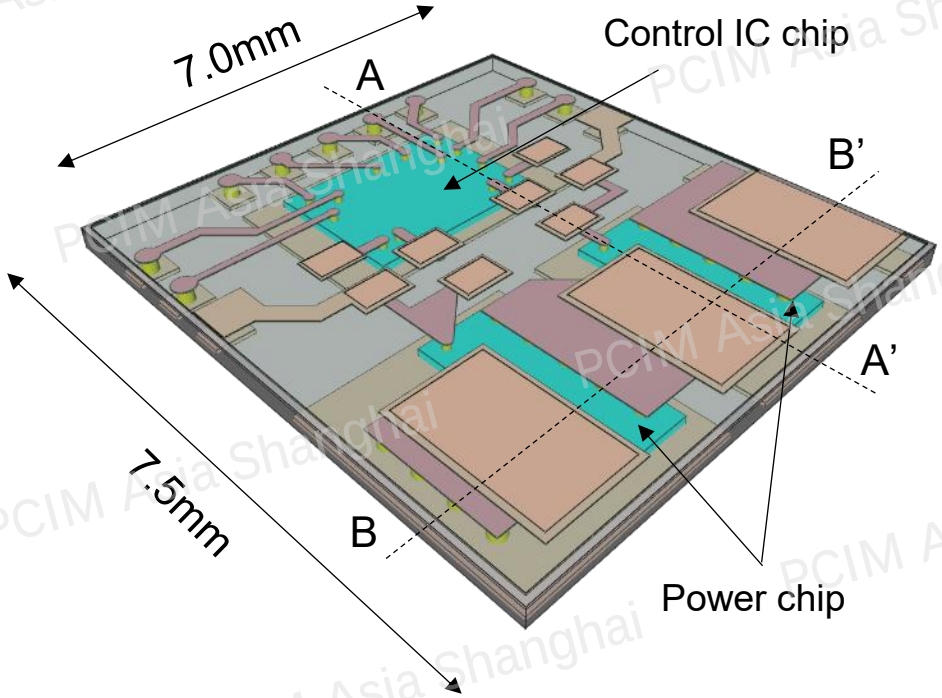




Panel warpage : 2mm Maximum

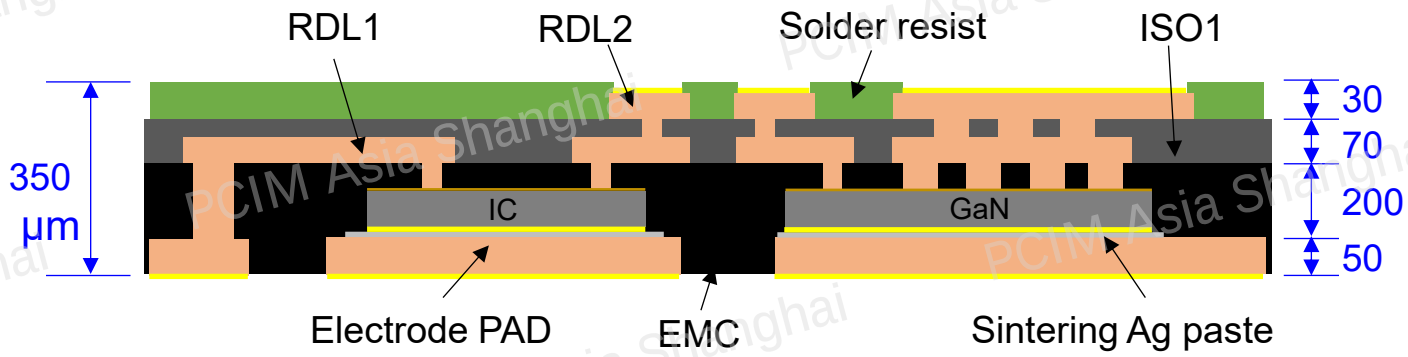
Package structure

■ Prototype package structure

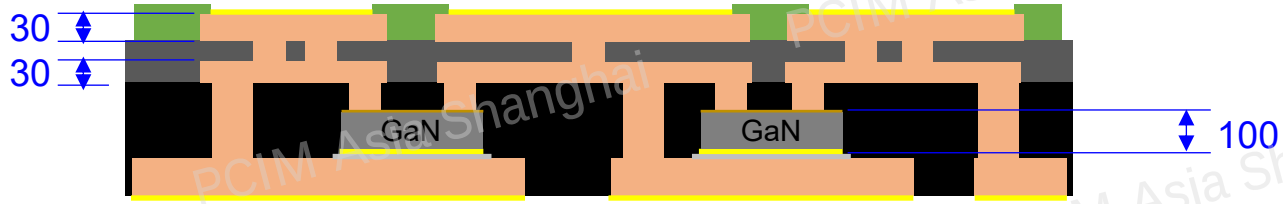


Control IC chip × 1, Power chip × 2

Design value /unit : μm



Cross-section A-A'



Cross-section B-B'

- Ultra-thin & high heat dissipation module with DC-DC half-bridge structure.
- Motif of GaN HEMT for power and high-speed switching.

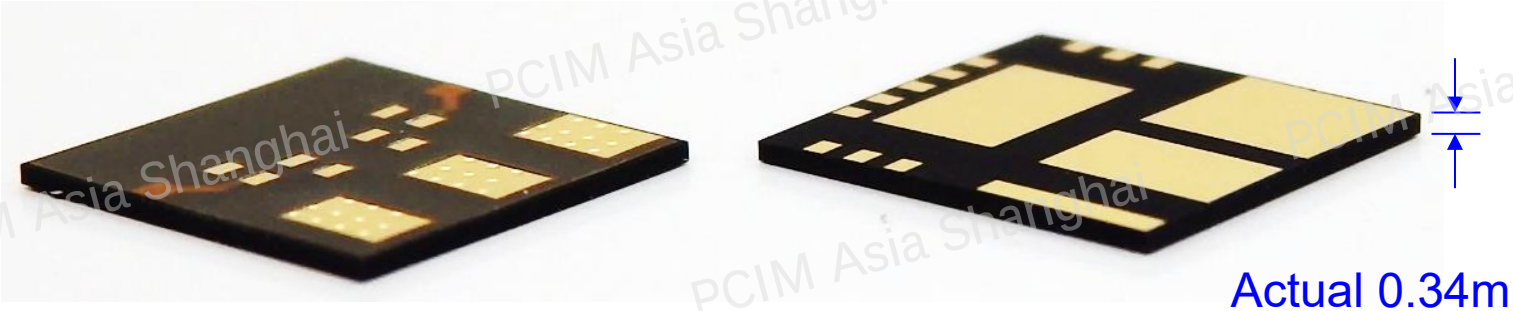
Package thickness & X-ray CT 3D image

- Prototyped package ***Package thickness***

New Coreless chip embedded module package

Top side

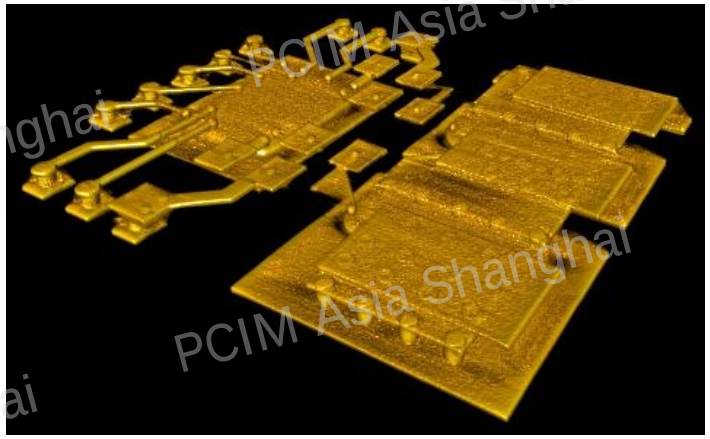
Bottom side



Actual 0.34mm

Package size : 7.0×7.5mm

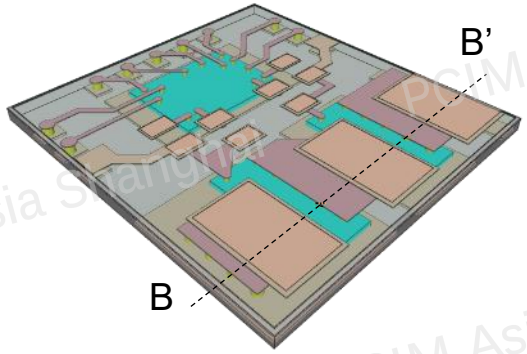
X-ray CT 3D image
(Internal structure)



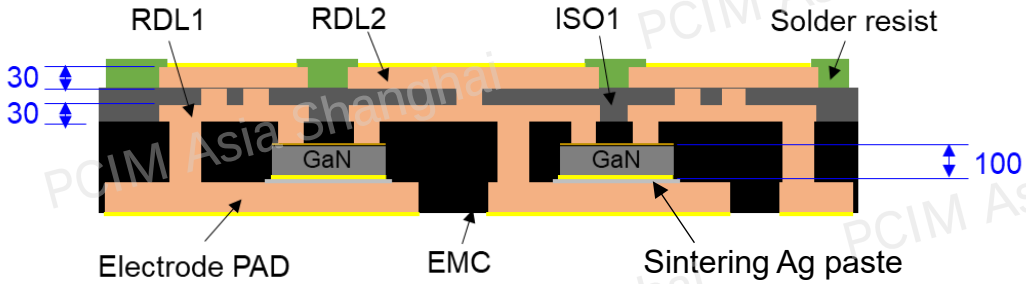
Our proposed new Coreless chip embedded package thickness is actual 0.34mm.
It is very thin compared to conventional power QFN.
Very thin SoC-like analog and power module package such as heterogeneous chip bonding can also be realized.

Package Cross-section

- Prototyped package



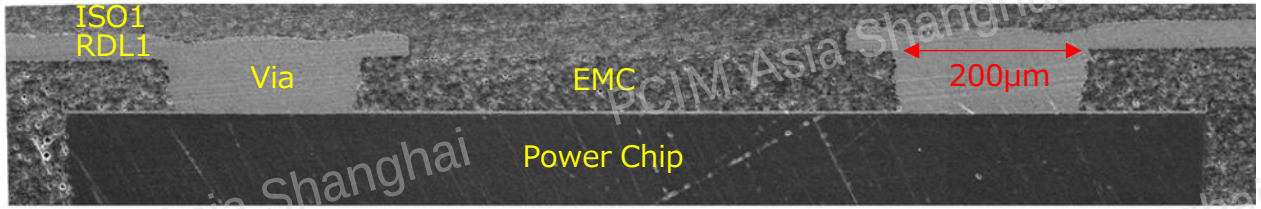
Cross-section SEM image



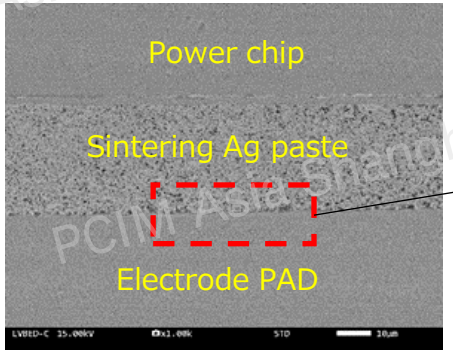
Cross-section B-B'

Actual Cross-section B-B'

Direct Cu plating connection of power chips

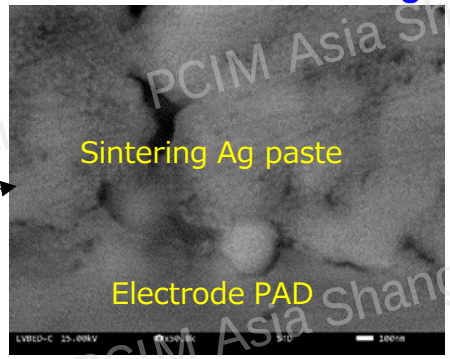


Chip attached paste



×1,000

Good Necking



×50,000

Warpage (coplanarity) evaluation result of package level

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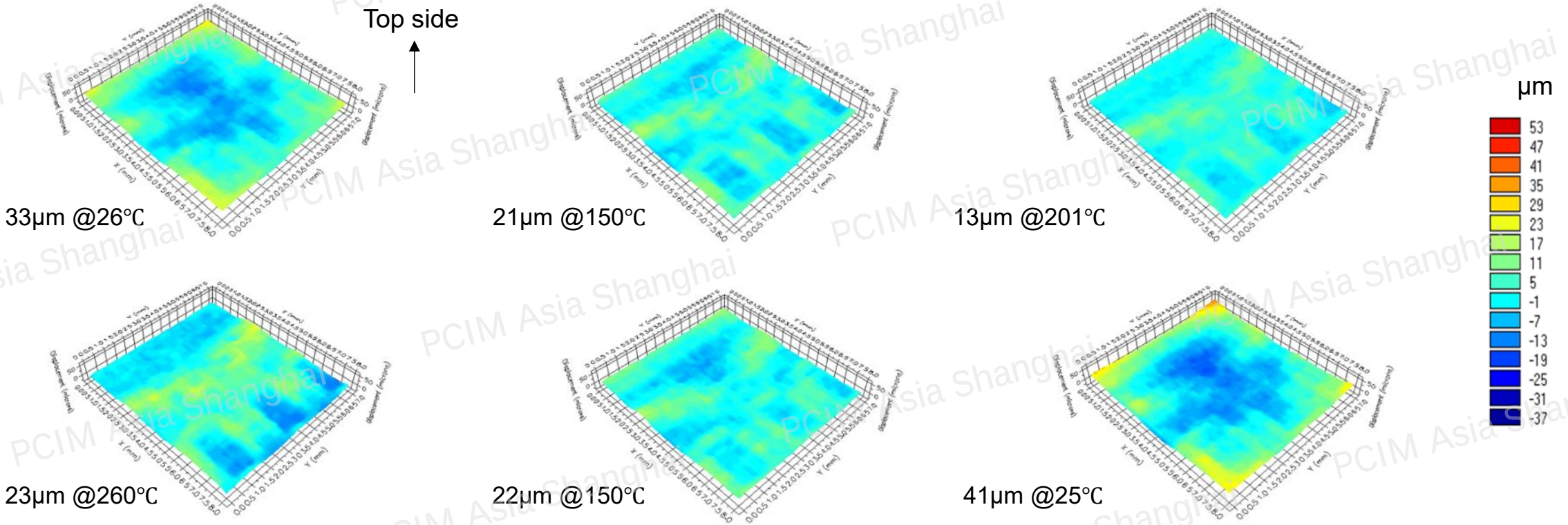
■ Package warpage

Warpage Behavior in the Reflow Temperature Range using shadow moiré method (3D Plot)



At room temperature, warpage was maximized (less than 50μm) with smile shape.
At high reflow temperature, warpage became small, tended to be flat.

Thin Multi chip power module for Chiplet integration device application

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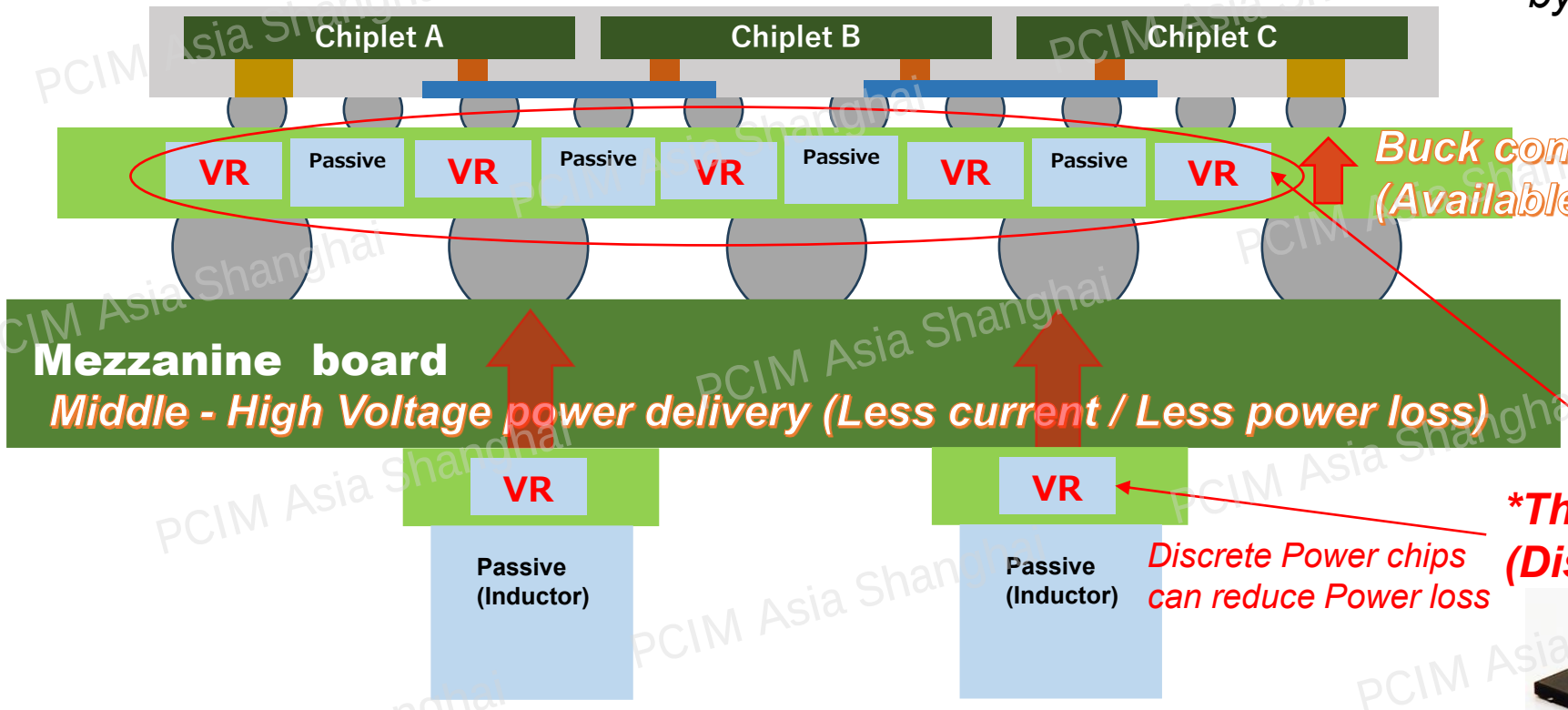
- Suitable power delivery by IVR (Integrated Voltage Regulator)



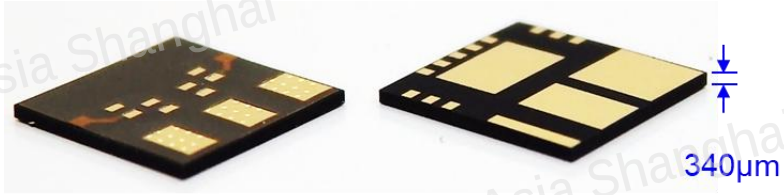
Each unit can be controlled by the appropriate voltage

Buck convert to appropriate voltage (Available for multi-voltage rail)

*High speed SW **VR** can reduce the **Passive** (inductor) size !*

Thin Multi chip voltage regulator (Discrete Power + controller chip)

Discrete Power chips can reduce Power loss



Package size : 7.0×7.5mm

Thin GaN HEMT voltage regulator with built-in inductor

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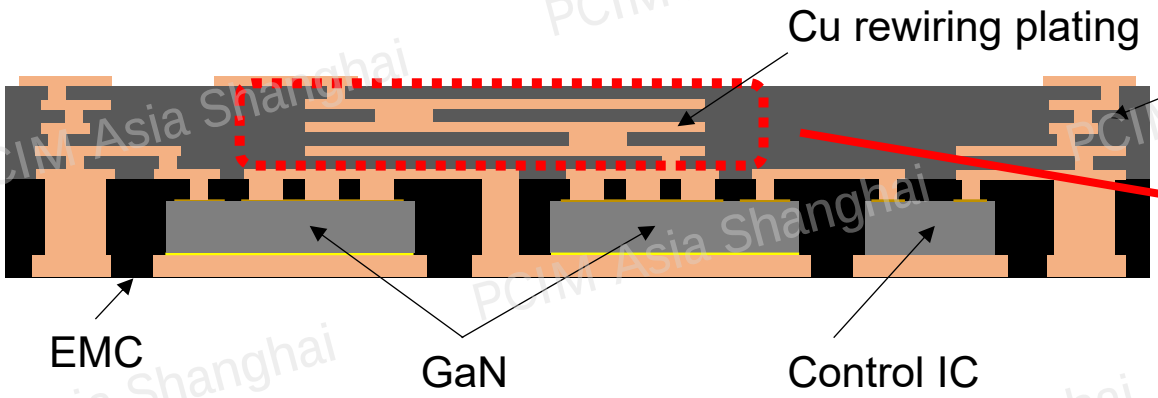
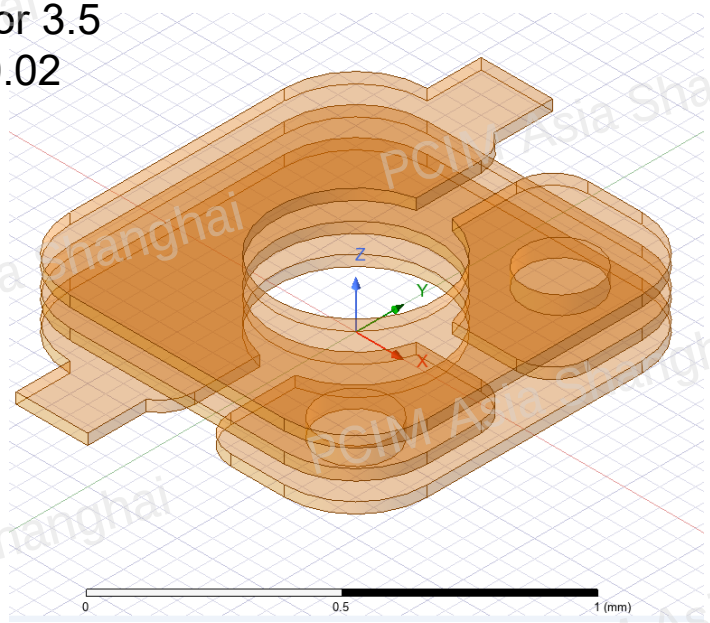
- **GaN HEMT voltage regulator with a built-in inductor formed by Cu rewiring plating (RDL)**



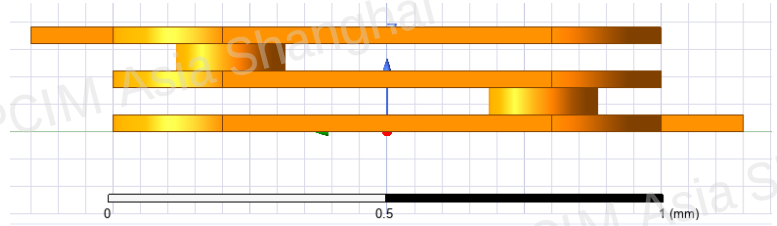
Dielectric layer
μ=1.0 or 3.5
tanδ=0.02



Vertical structures (Cu plating (RDL) & Isolation layers)

u=1/1/1	u=1/3.5/1	u=1/3.5/3.5	u=3.5/3.5/3.5	
u=1	u=1	u=1	u=3.5	50umt
Copper	Copper	Copper	Copper	30umt
u=1	u=3.5	u=3.5	u=3.5	50umt
Copper	Copper	Copper	Copper	30umt
u=1	u=3.5	u=3.5	u=3.5	50umt
Copper	Copper	Copper	Copper	30umt
u=1	u=1	u=3.5	u=3.5	50umt

290 μm



30
50

Source : APEC 2025 AOI

Simulation vs Prototype measurement results

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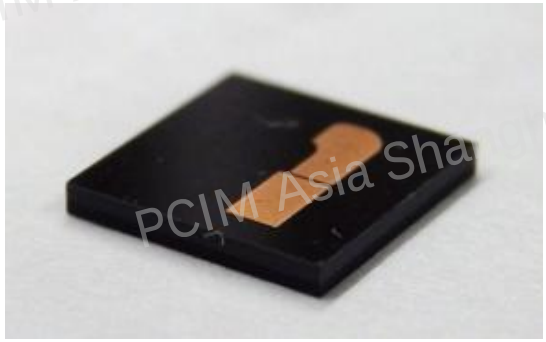
■ Inductance

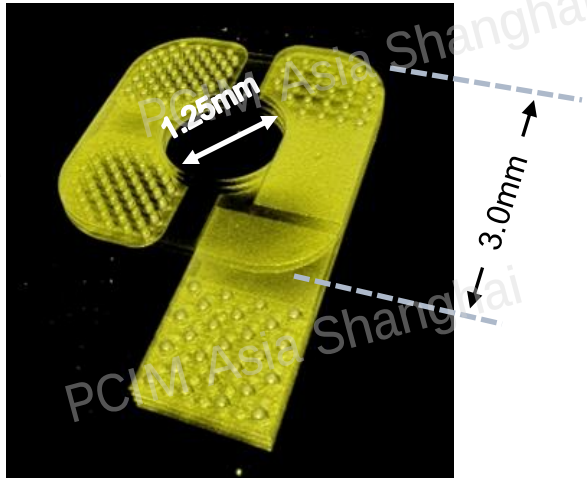
Simulation vs Prototype results

Structual conditions

- ▶ Inductor size : 3.0mm □
- ▶ Inner hole diameter : 1.25mm
- ▶ Frequency : 100MHz
- ▶ Vertical structures (RDL & Isolation)

⇒ Fig.8





Prototype Photo & X-ray CT 3D image

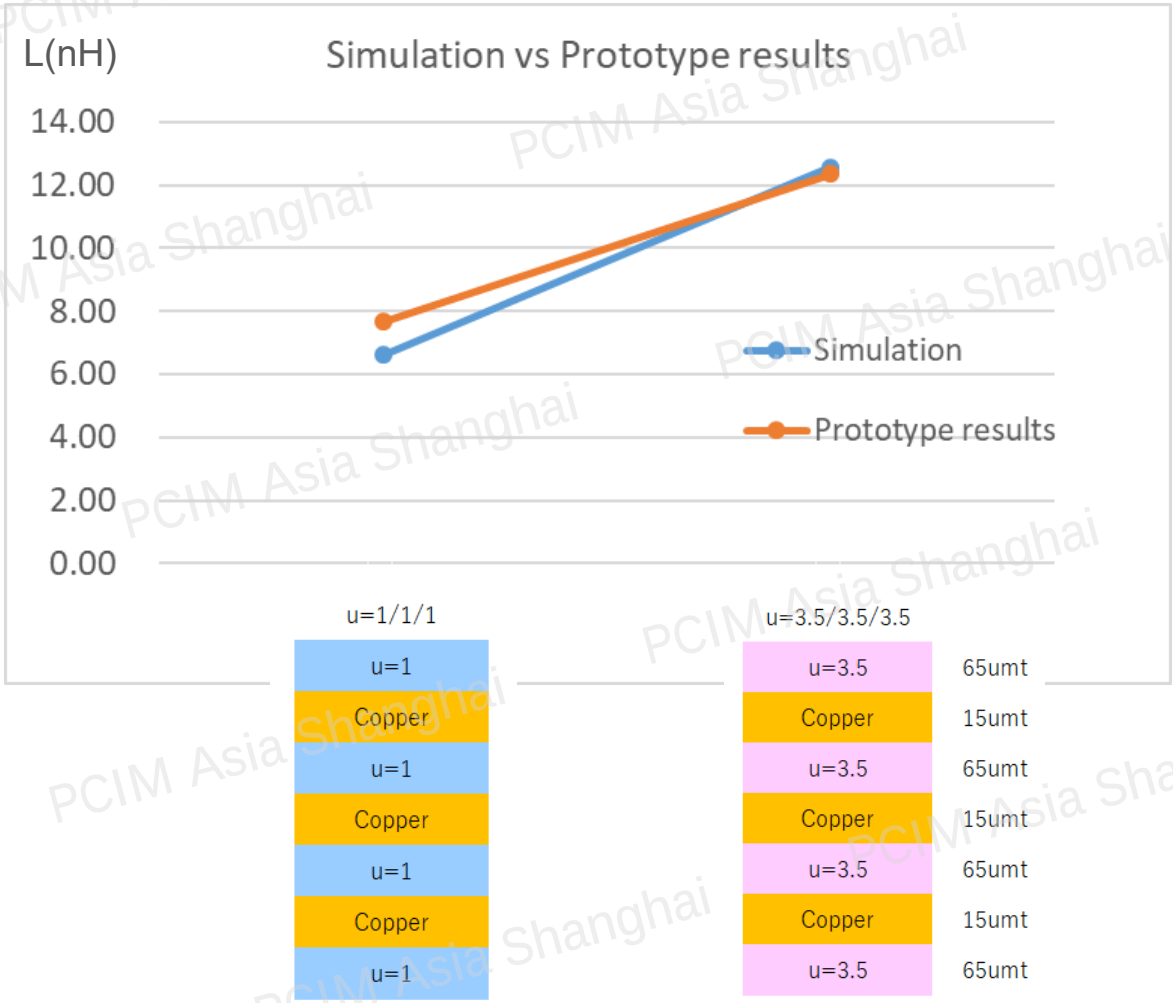


Fig.8 RDL structure

Thin GaN HEMT voltage regulator with built-in inductor (PoC)

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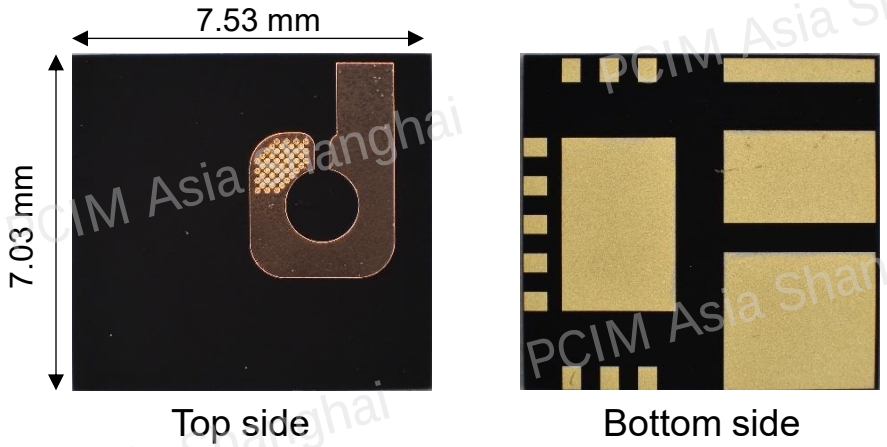
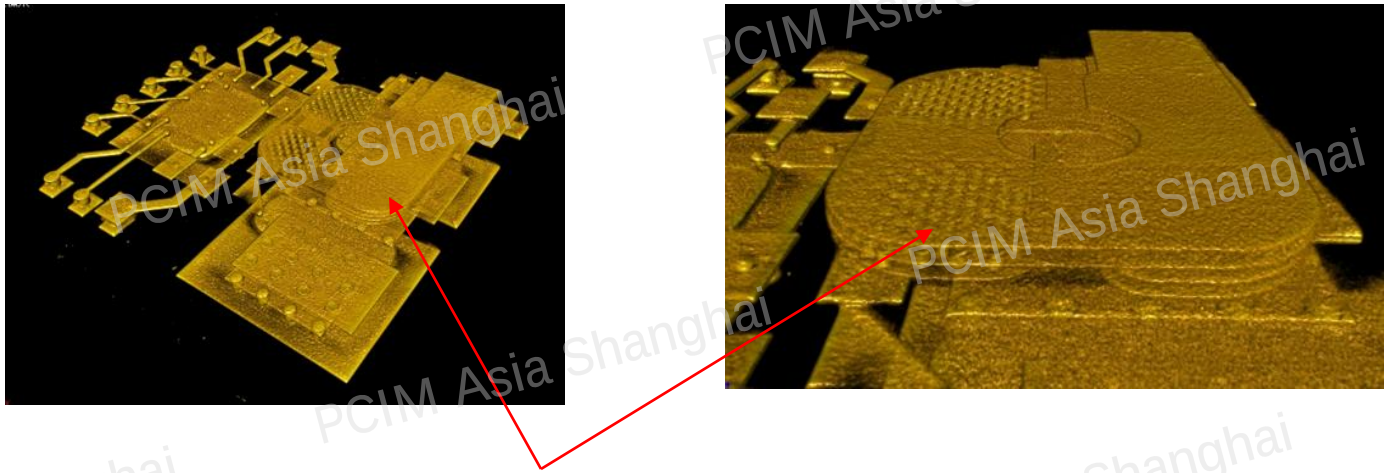
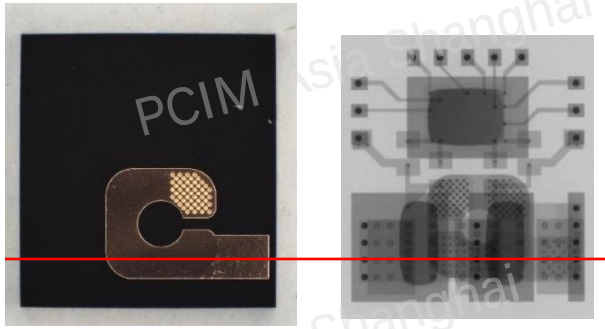
Prototype package outline



X-ray CT 3D image



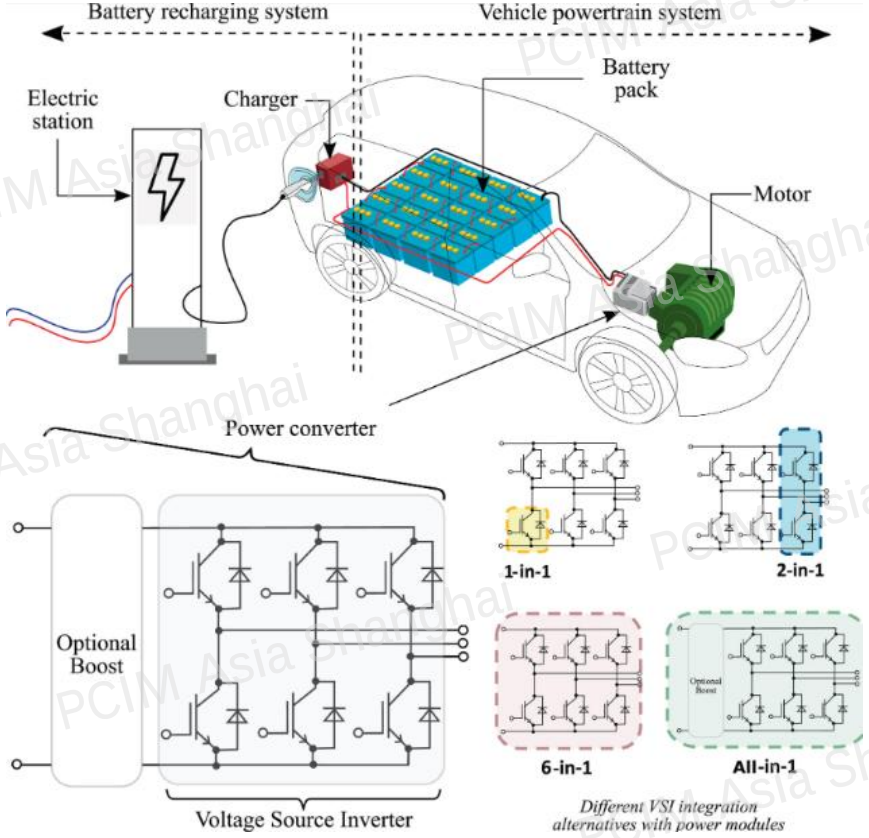


Chip Embedded Power Package for Automotive applications

Source : TOYOTA corporation

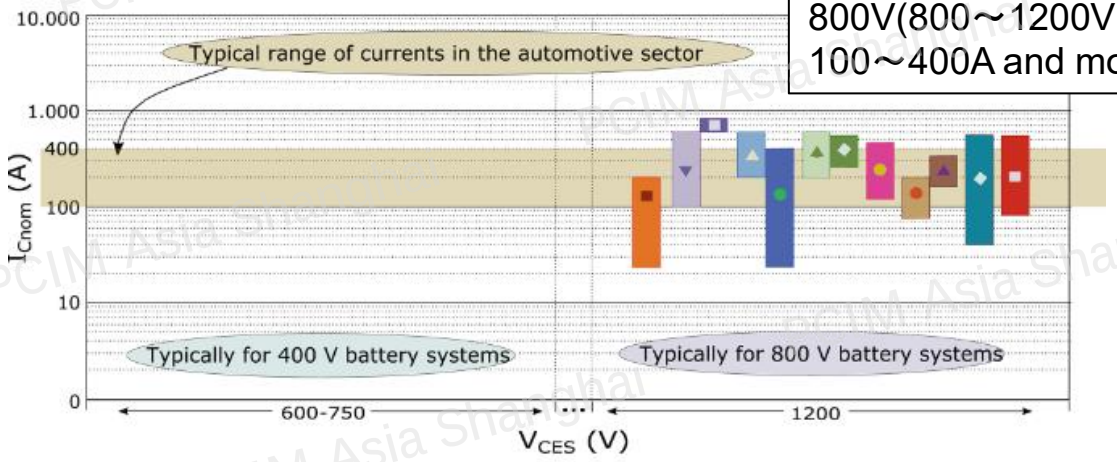
SiC inverter module

EV traction inverters

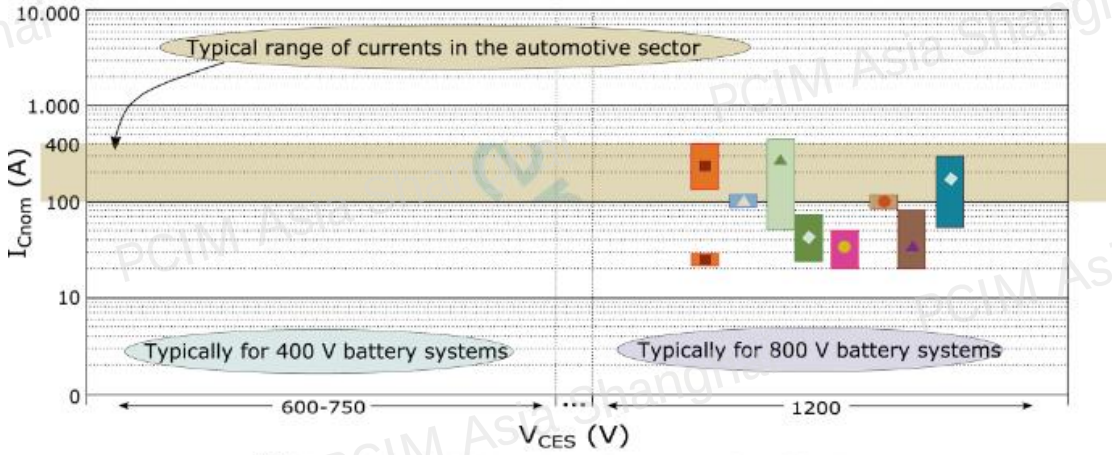


Source：
https://onlinelibrary.wiley.com/doi/full/10.1002/er.8581
The role of power device technology in the electric vehicle powertrain

EV battery bus voltage
800V(800～1200V)
100～400A and more



(A) Modules for the Half-Bridge topology (2-in-1).



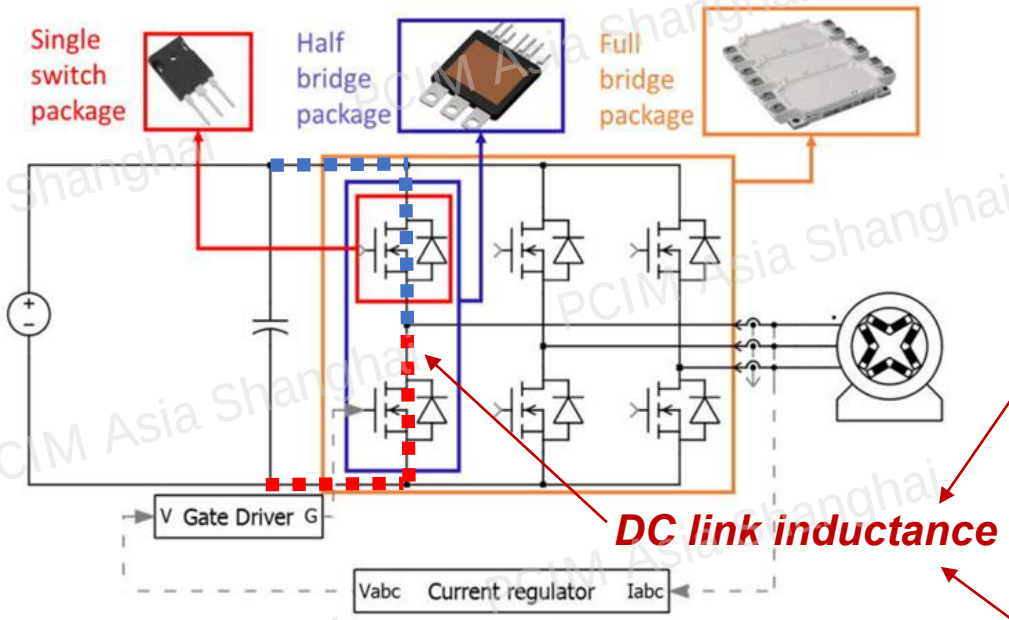
(B) Modules for the Voltage Source Inverter topology (6-in-1).

Source：
https://onlinelibrary.wiley.com/doi/full/10.1002/er.8581
The role of power device technology in the electric vehicle powertrain

Power Module Packaging Technologies

Several SiC inverter modules (packages) have been proposed, but further concept development is needed in terms of heat dissipation, high current, parasitic resistance, inductance and scalability.

Current module (package) trends



Source：IEEE/Comprehensive_Review_and_State_of_Development_of_Double-Sided_Cooled_Package_Technology_for_Automotive_Power_Modules

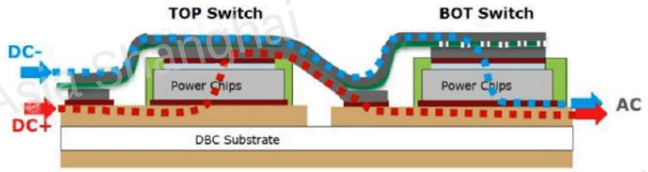
Case module (package) type

- *High customizable package design*
- *Complicated wiring*
- *Thinning down is limited due to wire loops*
- *High parasitic inductances due to long wire loops*
- *Wire bonding junction failure in reliability*

Discrete type

- *Larger mounting space*
- *Need many packages (Cost)*
- *High parasitic inductance*

Parasitic inductance of each module



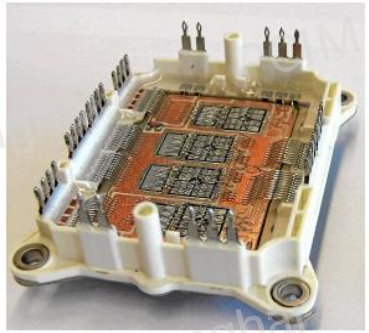
eMPack® module stray inductance ~2.5 nH
~ 6 nH incl. capacitor (eMPack® ref. design)

Source : Semikron Danfoss Webinar : eMPack Power Module Family

Chip Embedded Technology can make the DC loop very short to reduce parasitic inductance (< 1nH)

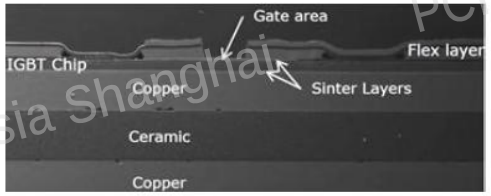
Power Modules
Towards Planar Power

Conventional Module



Wire Bonds (Al or Cu)
➔ **30 - 100 nH**

Semikron Danfos - eMPack®



SKiM® technology – flex on top
➔ **2.5 nH**

Embedding Module

Flat PCB Cu wiring on top
➔ **0.5 nH**

Source : NEPCON Japan 2025 Fraunhofer IZM

Panel Level chip embedded technology

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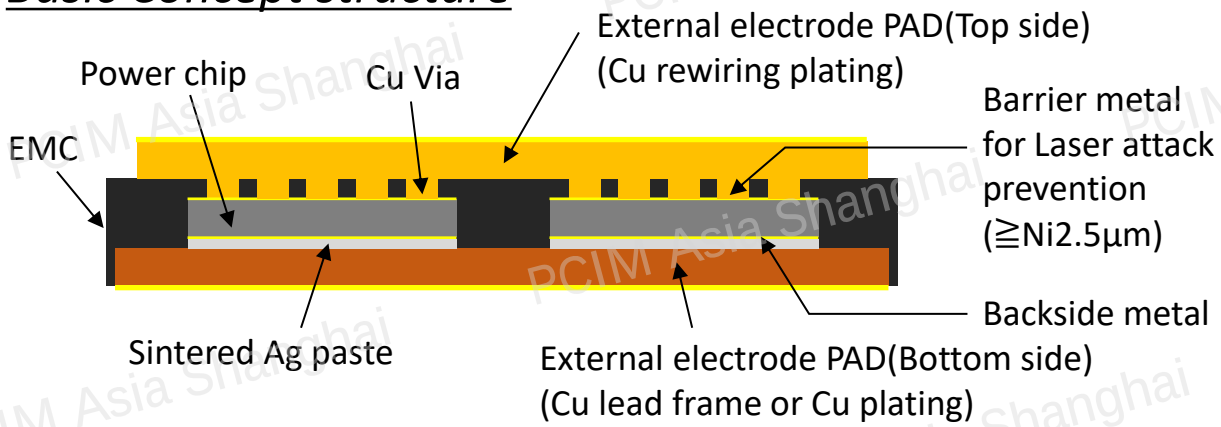
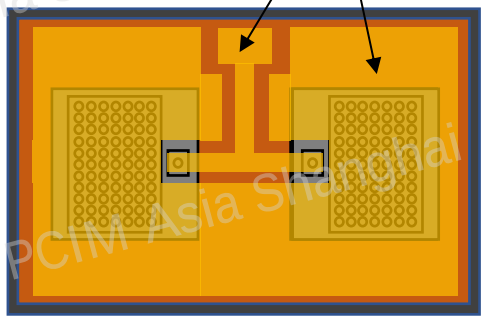
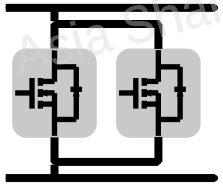
Proposal for Core Power Module Package using chip-embedded technology with high scalability for inverter applications

Basic Concept structure



<Top view>





Power chip
Parallel connection ;
2, 3, … N parallel

Features

- Core power module package uses a semi-additive fan-out panel-level process (FOLP ® technology) customized for power applications.
- Cost-effective 300 mm square panel manufacture format.
- Uniquely epoxy coreless substrate and chip embedding technology.
- High current density by power chiplet like (chip parallel connection) technology
- Robust Cu-plated (Via and rewiring) interconnect technology.
- Enhanced High heat dissipation, High current density, low resistance and inductance.
- Integrated in-house production from panel substrate to package assembly.

Actual panel after molding
300 mm square panel format

Source : IMAPS ADVANCING MICROELECTRONIS Magazine 2024, Vol. 51, AOI

Interconnects Resistance Comparison

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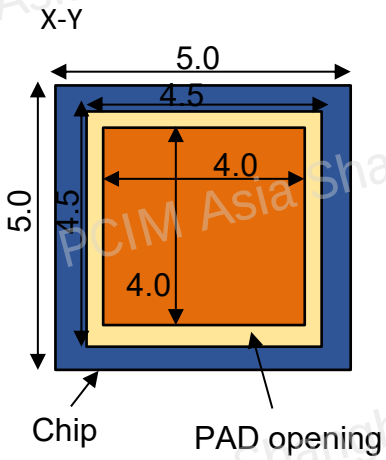
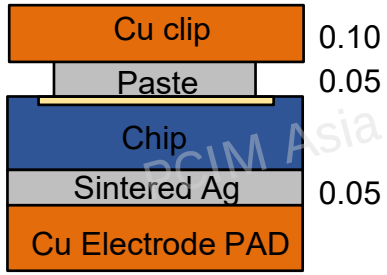
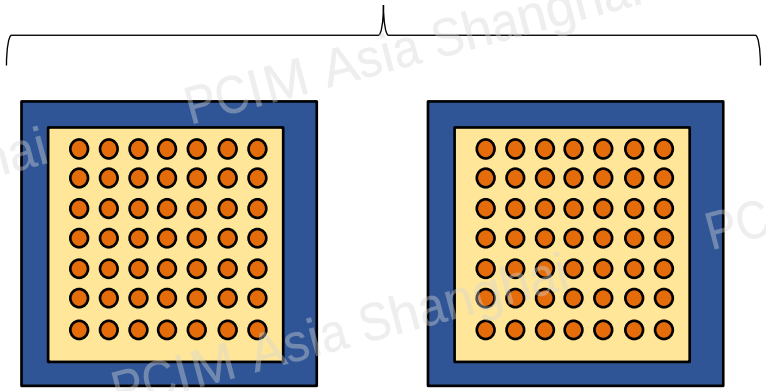
Conventional Cu clip type

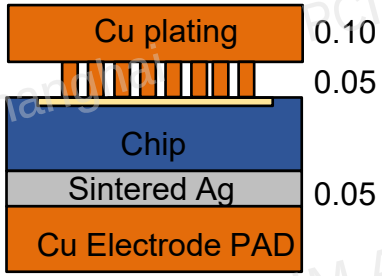




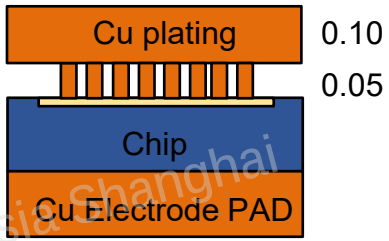
With Die Attach

Cu Via type





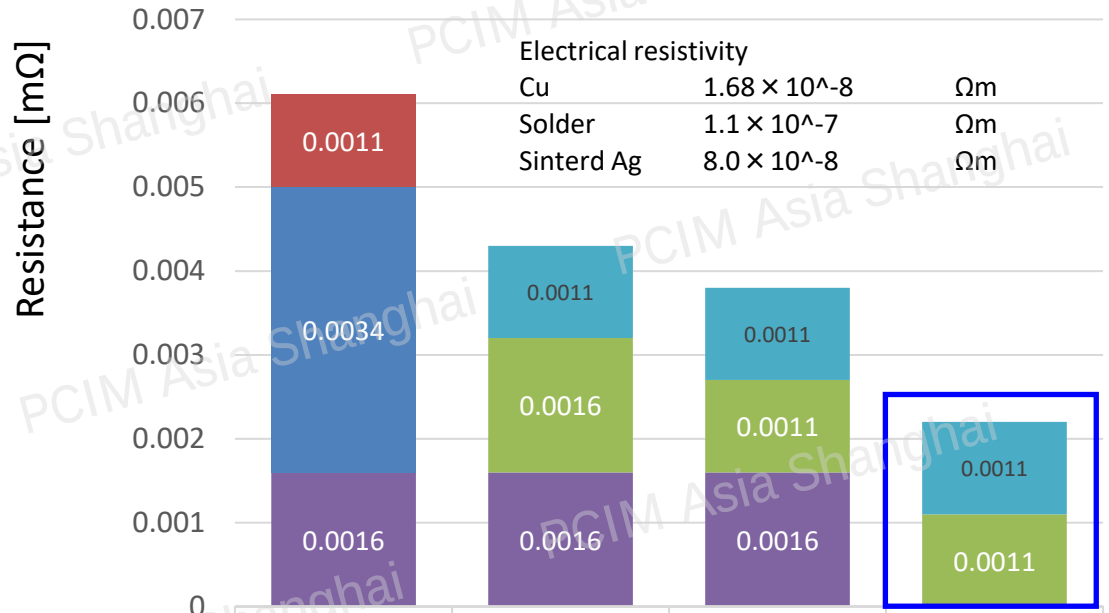
With Die Attach



Direct Cu bonding (Without Die Attach)

Unit : mm

Interconnects resistance (Theoretical calculation)



	Cu Clip with Die Attach	Cu Via with Die Attach Φ100μm	Cu Via with Die Attach Φ200μm	Direct Cu (without Die Attach) Φ200μm
⑤Cu plating(Chip top)		0.0011	0.0011	0.0011
④Cu Clip(Chip top)	0.0011			
③Cu Via(Chip top)		0.0016	0.0011	0.0011
②Solder(Chip top)	0.0034			
①Sinterd Ag(Chip bottom)	0.0016	0.0016	0.0016	

Chip and Cu Electrode PAD are not considered.

Panel Level chip embedded Core Power Module (SiC chip Direct Cu plating)

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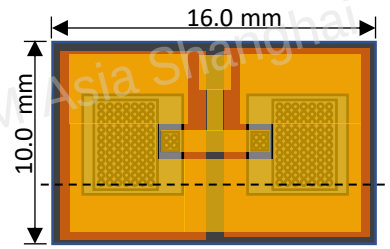
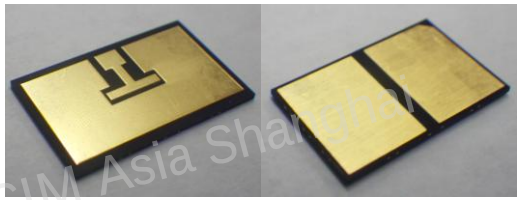
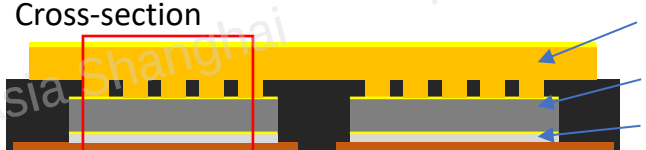
■ Technology Innovations in Core Module Packages

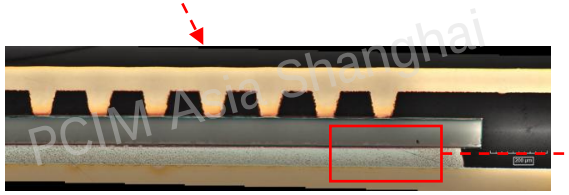
✓ Basic Technology (IMAPS DPC2024)

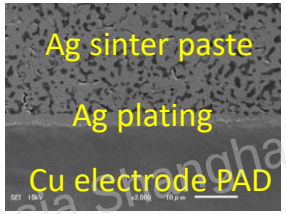
SiC chip Ag sinter bonding







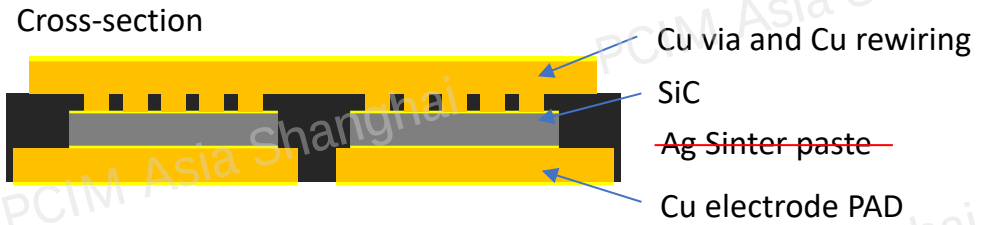




- Pressureless / pressure Ag sinter bonding
- Process issues :
  - BLT, spread, fillet, void control management
  - Optimization of sintering conditions (drying, pressurization, main sintering)

✓ New Technology (IMAPS APPE 2024)

SiC chip Direct Cu plating



<Motivations>

- Lower resistance and higher heat dissipation
- High Reliability Bonding with power chips
- No need for high temperature bonding process (reduced Cu surface oxidation)
- Miniaturization through chip-to-chip clearance reduction
- *Improved BLT, spread, fillet and void control issues (without die attach materials)*

Process Flow for Direct Cu Plating

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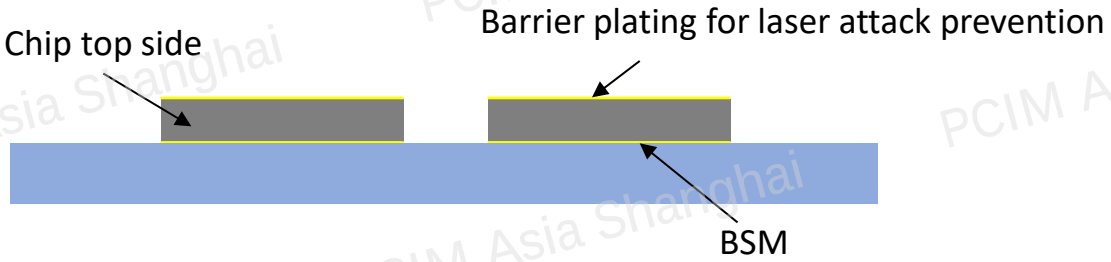
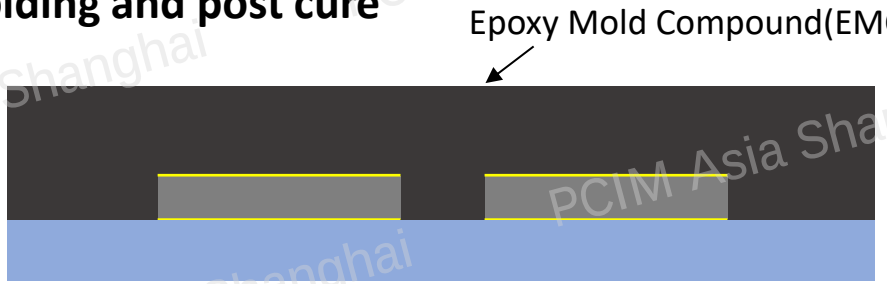
■ Process flow(Tentative)

1. Chip bonding on temporary carrier

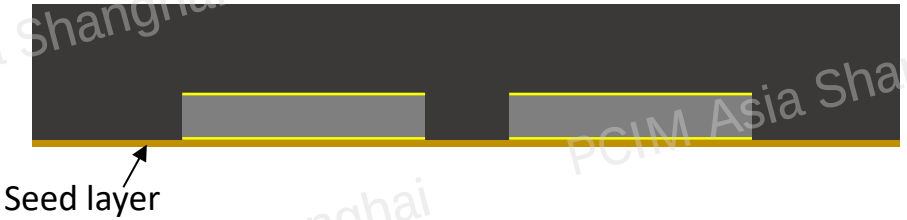


2. Molding and post cure



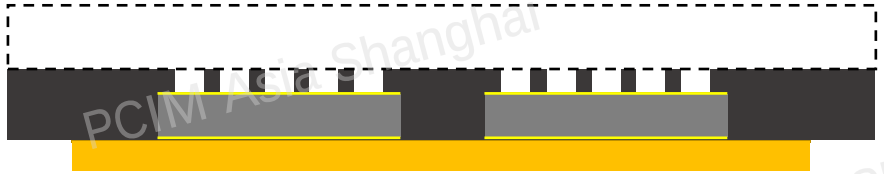
3. Temporary Carrier debonding

4. Seed layer formation



5. Electrode PAD formation with Cu plating

6. EMC(top side) grinding and Laser via drill on chips



Process flow for Direct Cu plating

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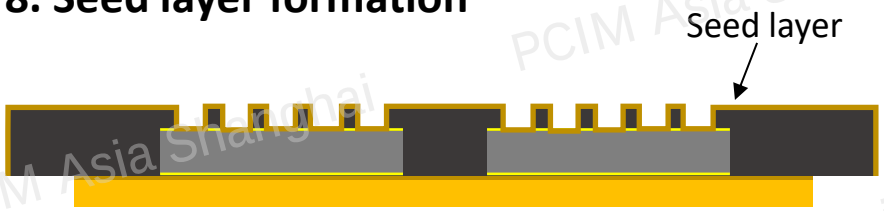
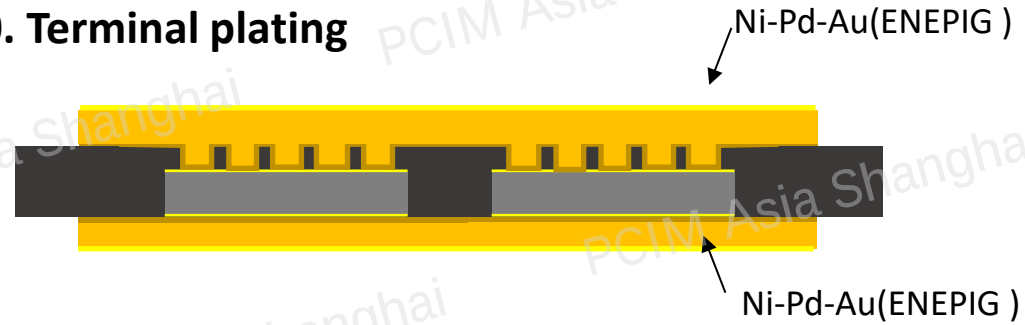
Process flow(Tentative)

8. Seed layer formation

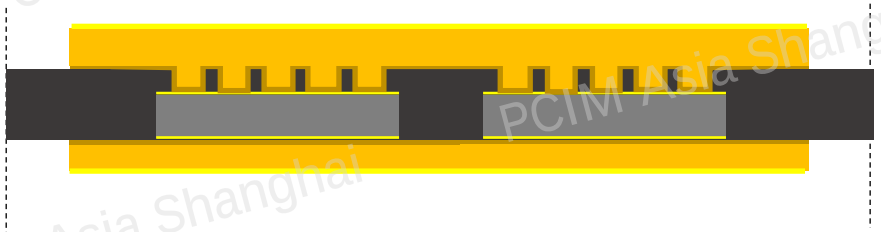


9. Via fill and Rewiring with Cu plating

10. Terminal plating

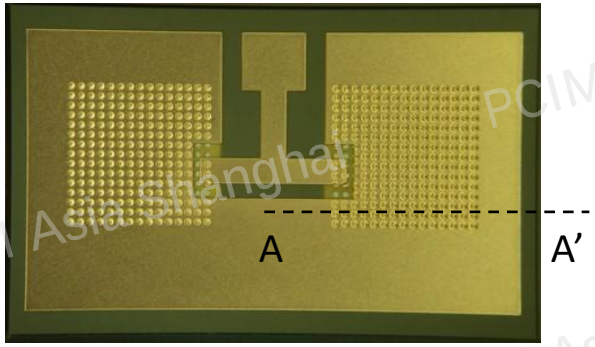


11. Singulation and finished

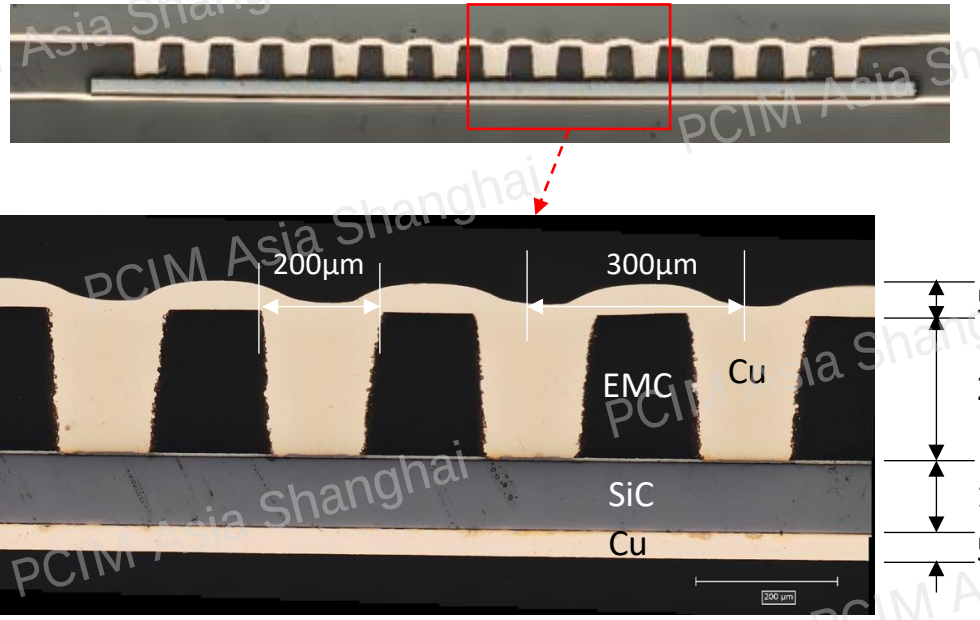


Results of Prototype Sample

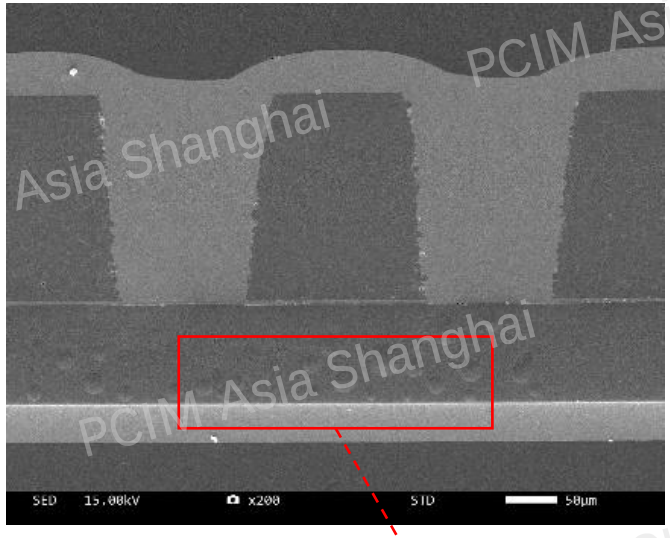
External view of prototype sample

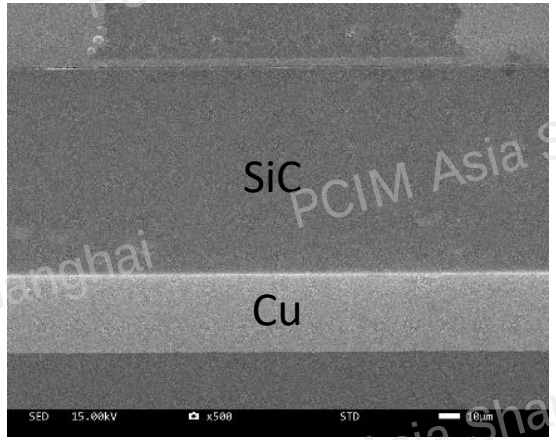


A-A' Cross-section by Microscopic photograph



Interconnects detail by SEM photograph





SiC-Cu Good bonding

Prototyping and Reliability Test Results

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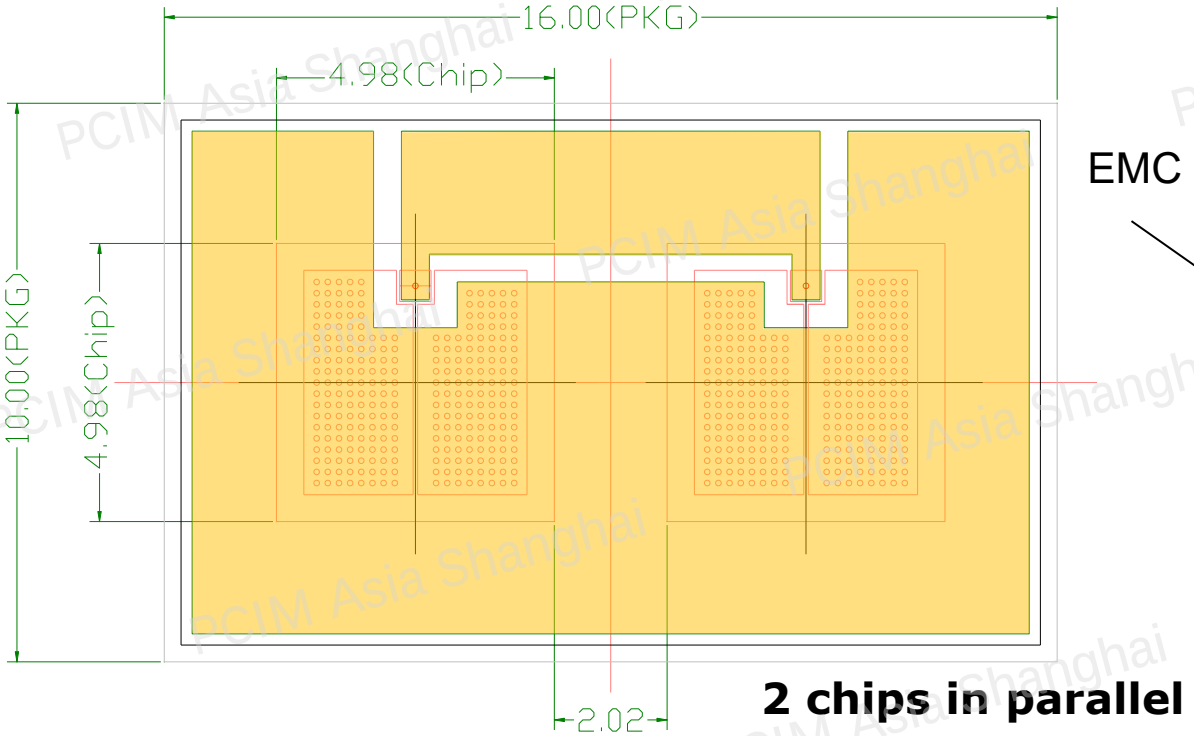
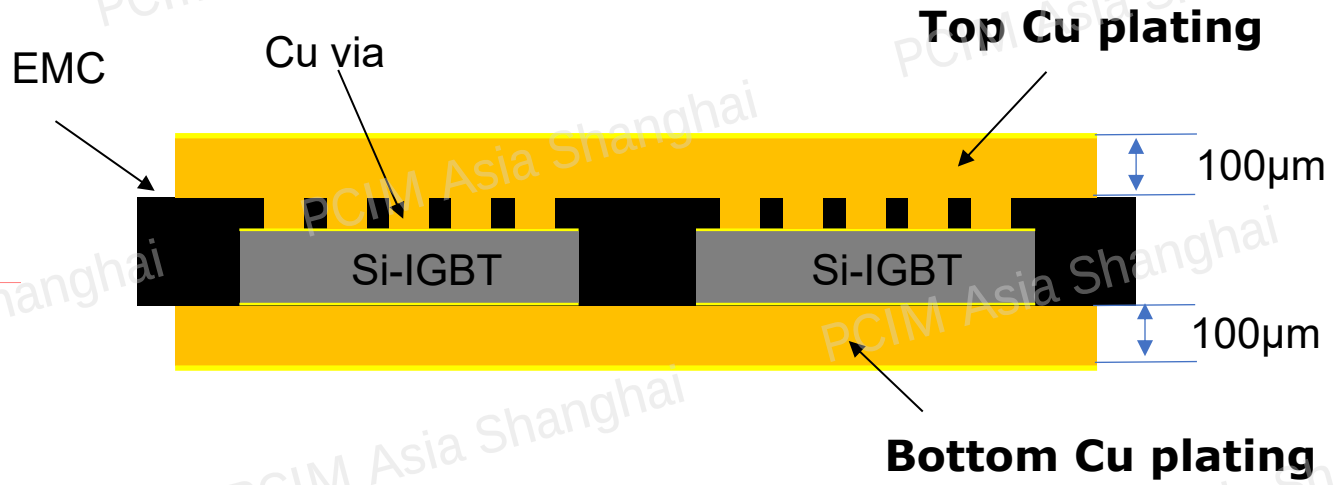
■ Package Design of Inverter for EVs



2 chips in parallel



Prototyping and Reliability Test Results

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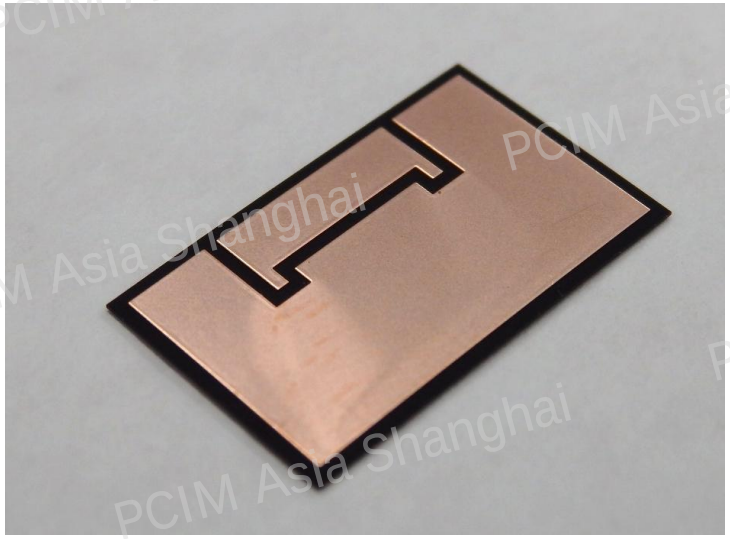
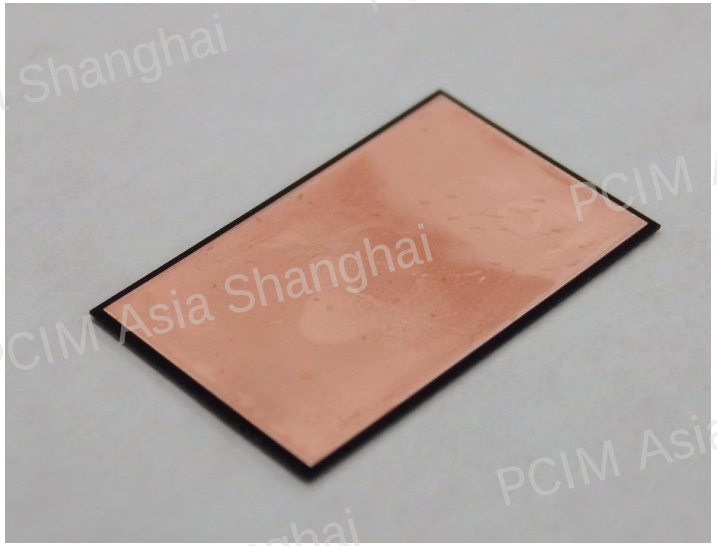
■ Finished Prototype

Package external image

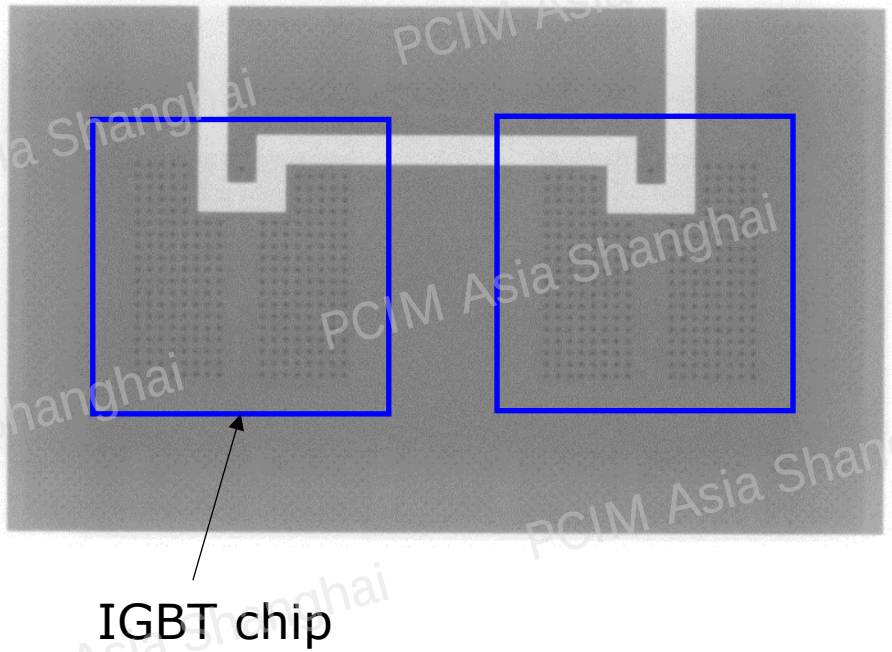
Top



Bottom



X-ray image



Power Cycling Test

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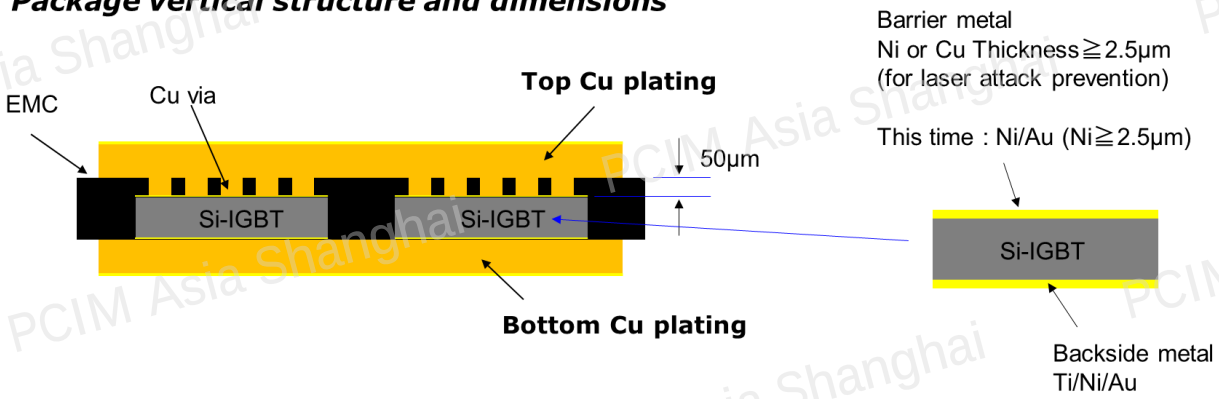
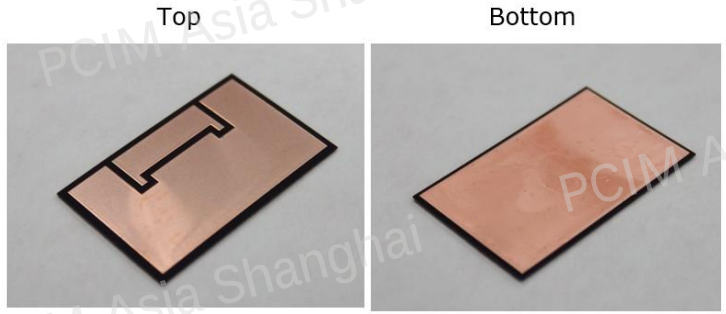
✓ ***Package vertical structure and dimensions***



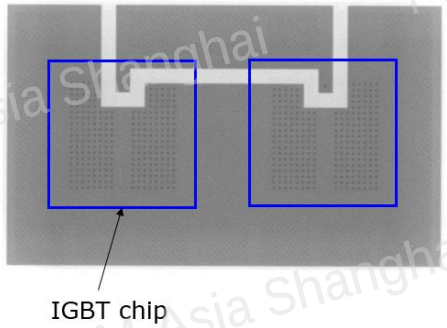
Level No.	Cu plating thickness(μm)	
	Top Cu	Bottom Cu
A	100	100
B	200	200

※Trial level

Package external image

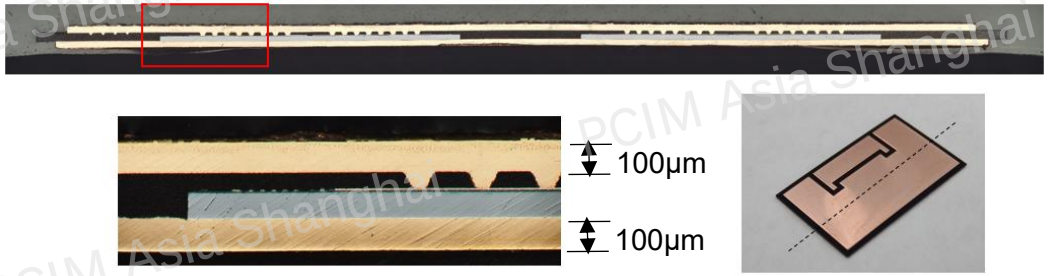


X-ray image

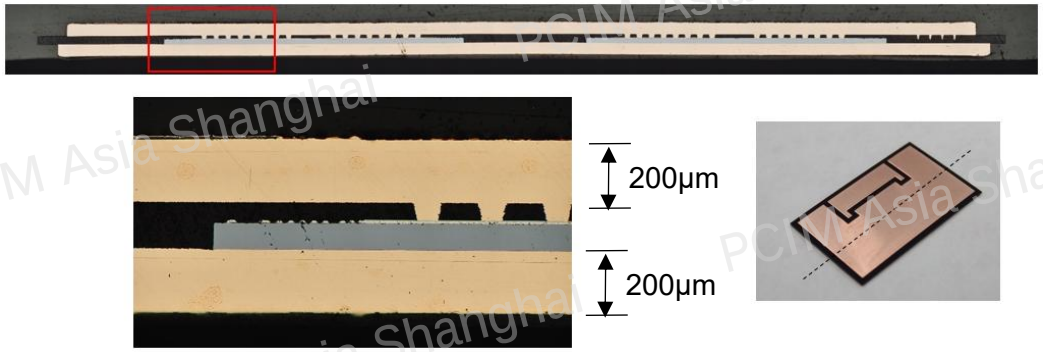


Cross-section image by microscope

Level No. A

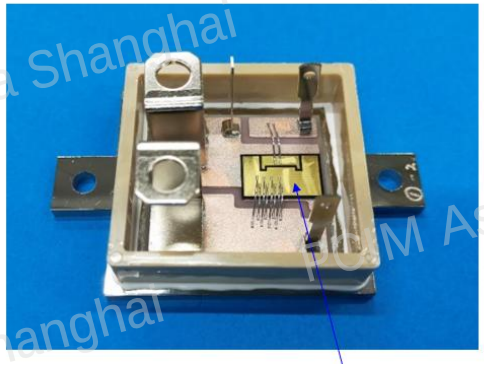


Level No. B

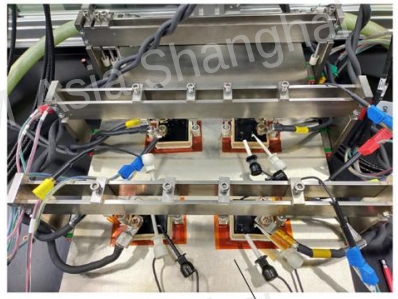


Power Cycling Test Sample structure

Before resin sealing

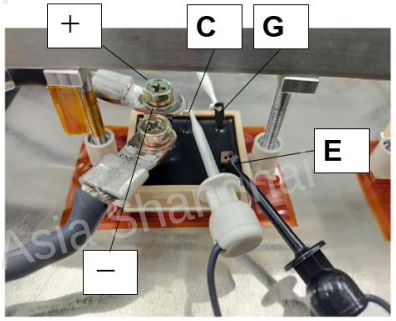


After resin sealing



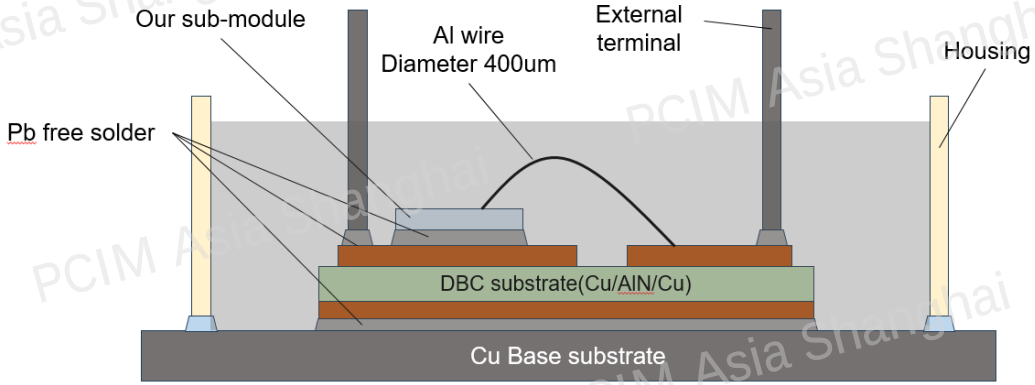
Cold plate

Outsourcing is used for testing (Chemitox, Japan)



+ : Input current
– : Output current
C : Collector
E : Emitter
G :Gate

Cross-section structure



Power Cycling Test

pcim
ASIA SHANGHAI

✓ ***Test conditions***

Items	Conditions
Test mode	Current constant mode : 45A(Between C-E terminal)
Cold plate temperature	25℃
Number of Si-IGBT chips	1 chip
ΔTj	A sample : 75℃ B sample : 65℃
ON/OFF time	ON=10sec OFF=20sec
Number of cycles	13,000 cyc

✓ ***Judgment items***

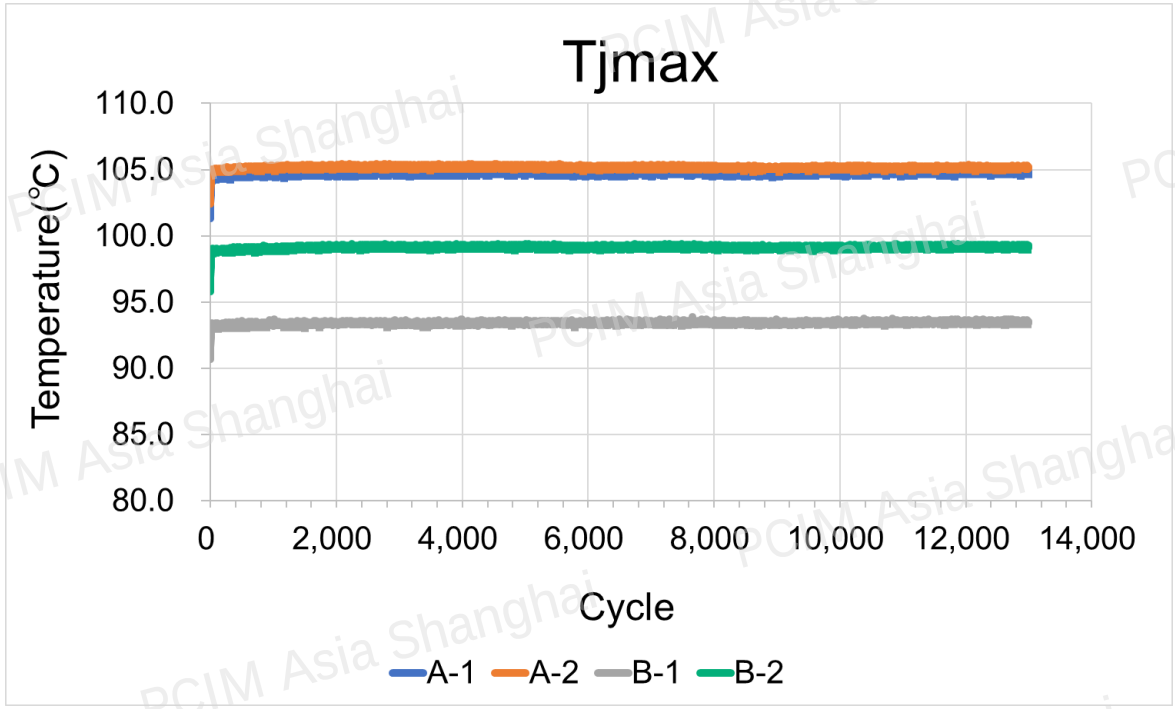
Items	Remarks(means)
Tjmax	Maximum temperature of chip when ON
Timin	Maximum temperature of chip when OFF
ΔTj	Tjmax-Tjmin
Von	On-voltage at current application

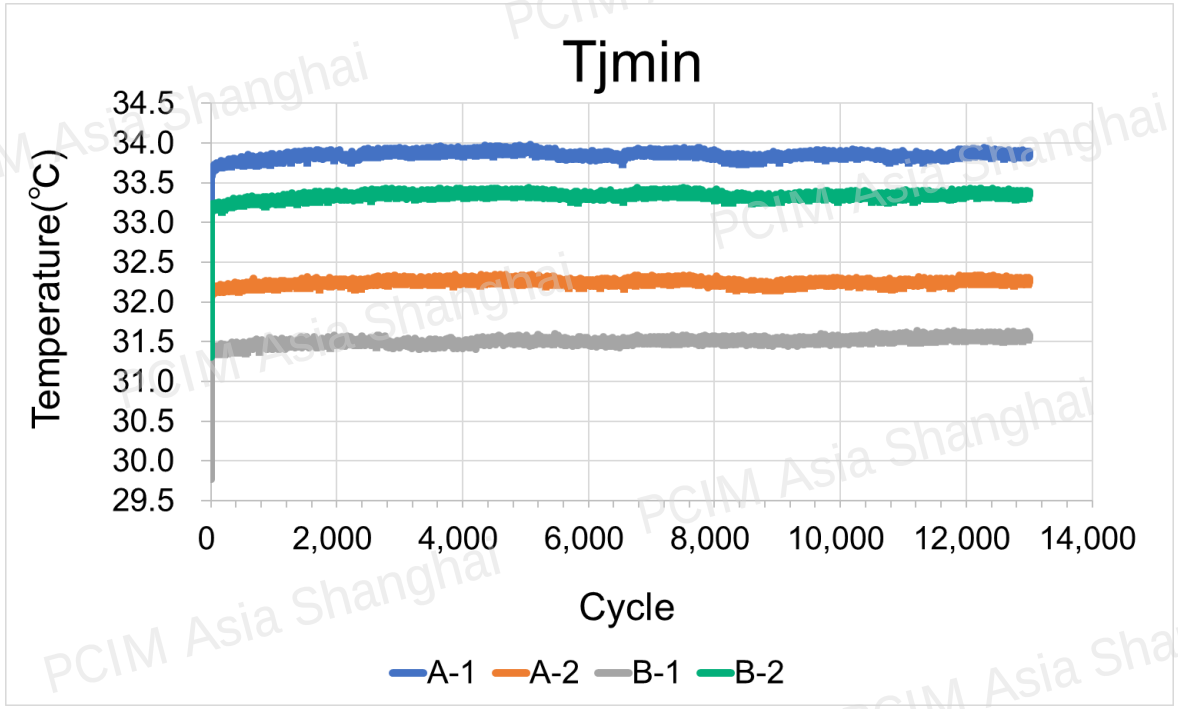
Power Cycling Test

pcim ASIA SHANGHAI

✓ ***Power cycling test results***

Sample A:Cu thickness 100μm
Sample B:Cu thickness 200μm





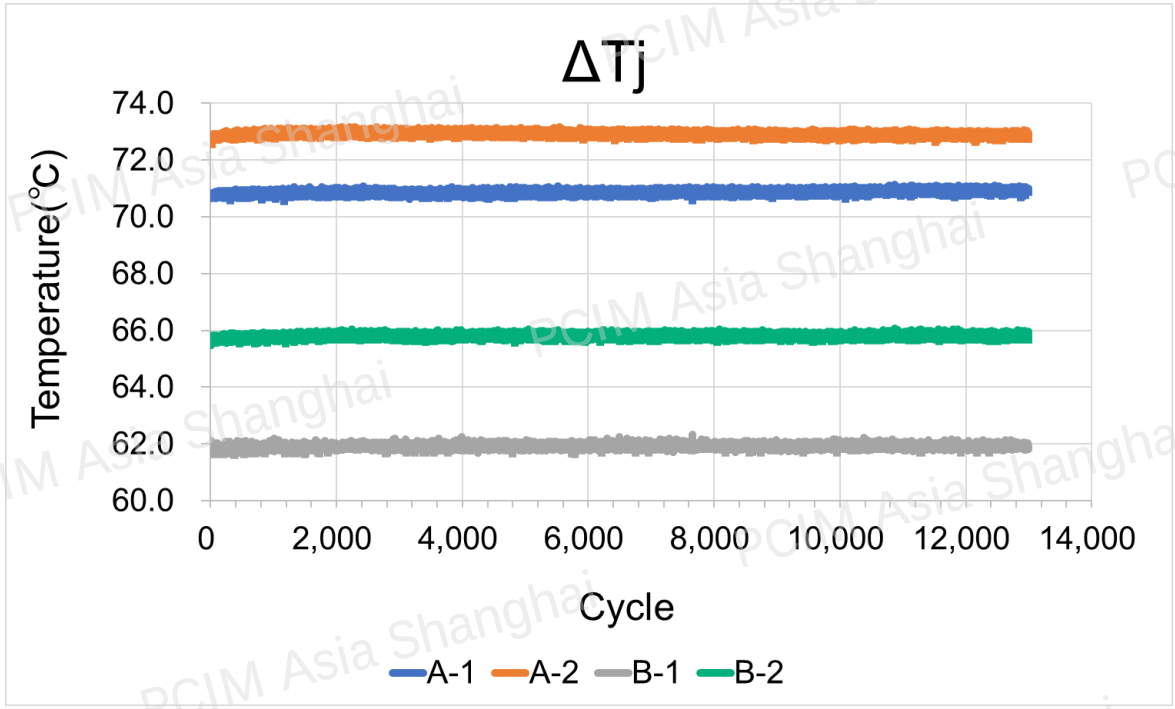
No characteristic change after 13,000 cycles

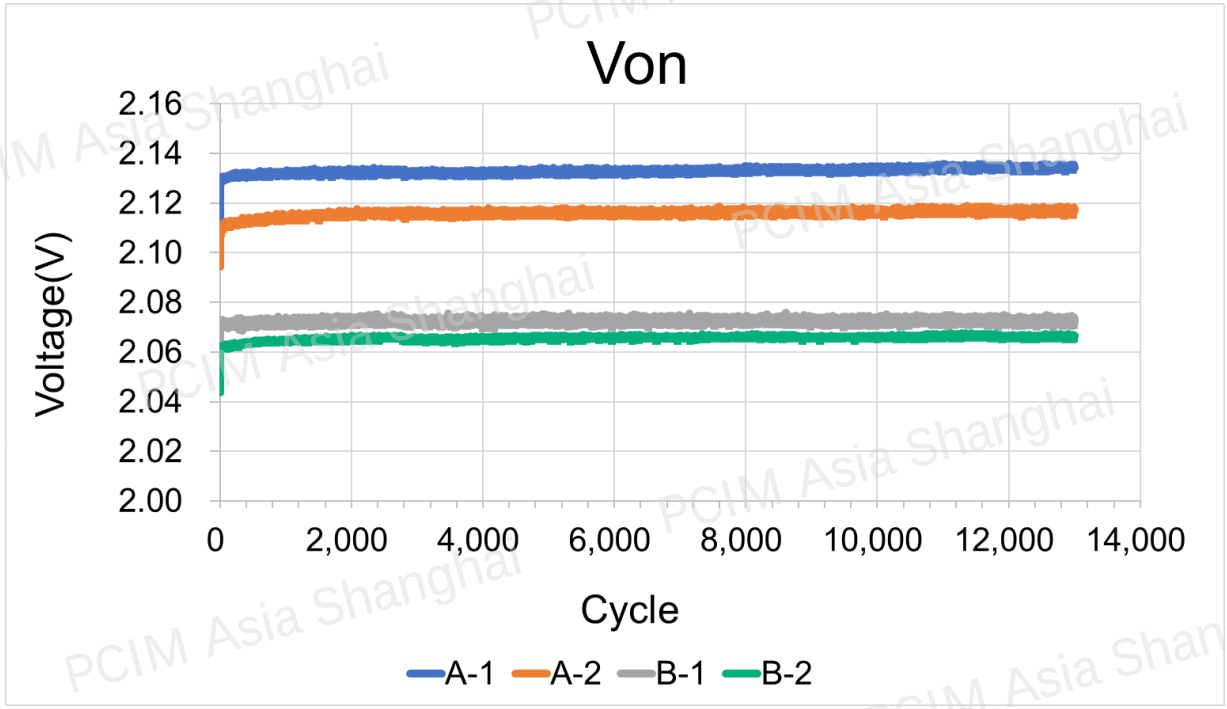
Good results

Power Cycling Test

✓ ***Power cycling test results***

Sample A:Cu thickness 100μm
Sample B:Cu thickness 200μm





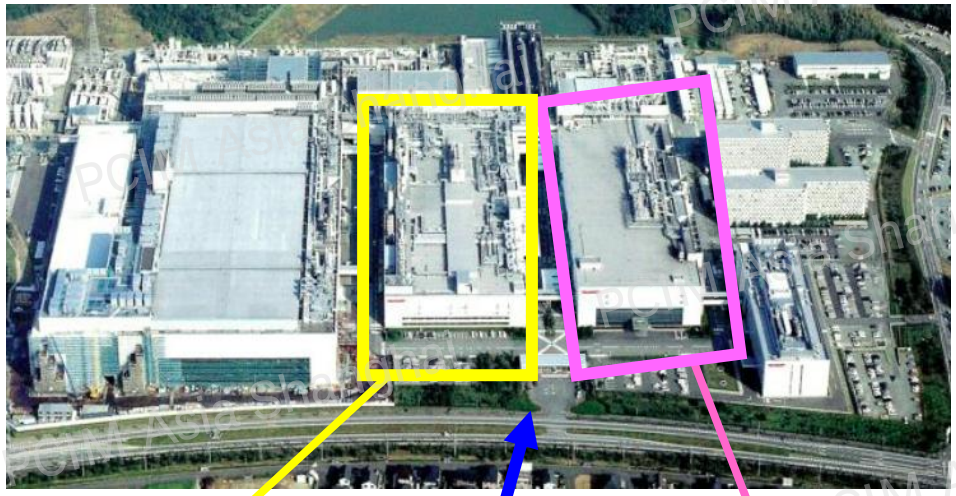
No characteristic change after 13,000 cycles

Good results

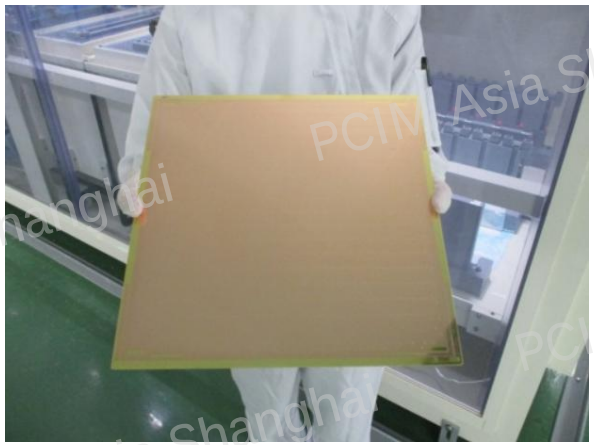
New Release: Panel manufacturing capacity expansion

NEWS RELEASE
31 July 2025

Regarding the Construction of the Production Line For Advanced Semiconductor Panel Packages at Sharp Mie Plant



By acquiring the second plant in addition to the first plant we already have, we will strengthen our ability to respond to new businesses, including the Advanced Packaging Business, with the aim of quickly launching a production line. At the same time, we will further accelerate the installation of necessary dedicated equipment and strengthening of our human resources structure, aiming to start full-scale operations in fiscal year 2027.



Going forward, by organically linking and optimizing the functions of both factories, we will aim to expand production capacity, streamline processes, and strengthen our supply system, thereby building a flexible and efficient production system that will enable us to respond more quickly to changes in market needs.

Summary

- ✓ There is an increasing market requirement for lower resistance and lower inductance, especially in the AI/data center and EV markets.
- ✓ Chip Embedded Technology is attracting a lot of attention due to the above market situation.
- ✓ Embedded Technology at the panel level is one of the most promising and realistic candidate.
- ✓ Regarding the AI/Data center market, the key is not only embedding the semiconductor chips but also embedding the passive components for high Power Integrity requirement.
- ✓ Regarding the EV inverter market, the key technologies are interconnection between the chip and metal base, as well as thick Cu RDL wiring. This reduces both electrical and thermal resistance and inductance, thereby improving efficiency.
- ✓ Reliability is the key issue, particularly with regard to interconnection between the chip and the metal, and delamination between each layer (e.g. chip/resin, Cu RDL/resin).

Thank you for your interest