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Dynamic Current Balancing Optimization of Cu Clip-Bonded SiC power module Based on Layout-Dominated Parasitic Inductance

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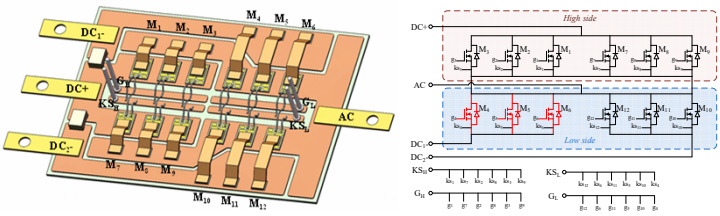
Introduction

Cu clip-bonding has lower resistance and lower inductance than wire-bonding, but unbalanced dynamic current still exists between paralleled silicon carbide (SiC) MOSFETs, limiting the available current capacity of Cu clip-bonded SiC power modules. This paper presents a parasitic inductance equivalent circuit model at switching transients, and a dynamic current balancing optimization guideline based on self- and mutual inductance of main current path segments is determined. The mismatch of the equivalent power source parasitic inductances is reduced by adjusting the bonding positions and shape parameters of Cu clips. Simulation results show that the dynamic current sharing performance is greatly improved.

Layout-Dominated Parasitic Inductance Equivalent Circuit Model



(a) DBC Layout (b) DBC topology

(c) Structural parameters of Cu clip

Fig. 1. Schematic of the baseline Cu clip-bonded SiC power module.

Baseline Cu Clip-Bonded SiC Power Module

- Each side switch consists of six paralleled SiC MOSFET dies with Kelvin-source connection;
- Due to the symmetry of the overall layout, this article only discusses the unbalanced dynamic current among low side dies M_4-M_6;
- The main structural parameters of Cu clip include span, height, thickness, and corner angle.

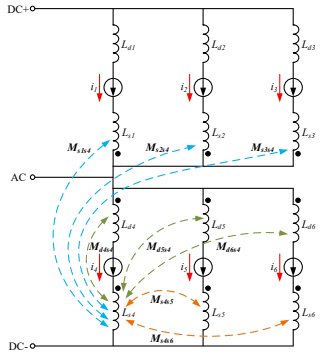


Fig. 2. Parasitic inductance equivalent circuit model at switching transients.

According to the DBC layout of the baseline Cu clip-bonded SiC power module, **the mutual inductance of the M_4 power source path segment can be divided into three main types** based on the criterion of tight magnetic coupling:

- M_{sis4} (i= 1, 2, 3)
- M_{dis4} (i= 4, 5, 6)
- M_{s4si} (i= 5, 6)

The parasitic inductance of dies M_4-M_6 can be represented with inductance matrices $\boldsymbol{L_1}$ and $\boldsymbol{L_2}$:

$$\boldsymbol{L_1}=\begin{bmatrix} M_{s1s4} & M_{s2s4} & M_{s3s4} \\ M_{s1s5} & M_{s2s5} & M_{s3s5} \\ M_{s1s6} & M_{s2s6} & M_{s3s6} \end{bmatrix} \tag{1}$$

$$\boldsymbol{L_2}=\begin{bmatrix} L_{s4}+M_{d4s4} & M_{d5s4}+M_{s4s5} & M_{d6s4}+M_{s4s6} \\ M_{d4s5}+M_{s4s5} & L_{s5}+M_{d5s5} & M_{d6s5}+M_{s5s6} \\ M_{d4s6}+M_{s4s6} & M_{d5s6}+M_{s5s6} & L_{s6}+M_{d6s6} \end{bmatrix} \tag{2}$$

According to the parasitic inductance equivalent circuit models, the induced voltage drops on M_4-M_6 power source path segments can be written as

$$\boldsymbol{v_{Ls}}=\begin{bmatrix}-\boldsymbol{L_1} & \boldsymbol{L_2}\end{bmatrix}\frac{d\boldsymbol{i}}{dt} \tag{3}$$

where $\boldsymbol{v_{Ls}}=\begin{bmatrix}v_{Ls4} & v_{Ls5} & v_{Ls6}\end{bmatrix}^T$, $\boldsymbol{i}=\begin{bmatrix}i_1 & i_2 & i_3 & i_4 & i_5 & i_6\end{bmatrix}^T$.

Balanced dynamic current among paralleled dies M_4-M_6 means that

$$v_{Ls4}=v_{Ls5}=v_{Ls6}=v_{Ls}' \tag{4}$$

$$\frac{di_1}{dt}=\frac{di_2}{dt}=\frac{di_3}{dt}=\frac{di_4}{dt}=\frac{di_5}{dt}=\frac{di_6}{dt}=\frac{di'}{dt} \tag{5}$$

Take (4) and (5) into (3), it can be derived that

$$\begin{bmatrix} v_{Ls}' \\ v_{Ls}' \\ v_{Ls}' \end{bmatrix}=-\begin{bmatrix} M_{s1s4}+M_{s2s4}+M_{s3s4} \\ M_{s1s5}+M_{s2s5}+M_{s3s5} \\ M_{s1s6}+M_{s2s6}+M_{s3s6} \end{bmatrix}\frac{di'}{dt}+\begin{bmatrix} L_{s4}+M_{d4s4}+M_{d5s4}+M_{s4s5}+M_{d6s4}+M_{s4s6} \\ M_{d4s5}+M_{s4s5}+L_{s5}+M_{d5s5}+M_{d6s5}+M_{s5s6} \\ M_{d4s6}+M_{s4s6}+M_{d5s6}+M_{s5s6}+L_{s6}+M_{d6s6} \end{bmatrix}\frac{di'}{dt}$$

$$=\boldsymbol{L_e}\frac{di'}{dt} \tag{6}$$

where $\boldsymbol{L_e}=\begin{bmatrix}L_{e4} & L_{e5} & L_{e6}\end{bmatrix}^T$. In order to satisfy (6), the equivalent power source inductances should be equal, which is also the **optimization guideline for the baseline clip-bonded SiC power module to achieve balanced dynamic current**.

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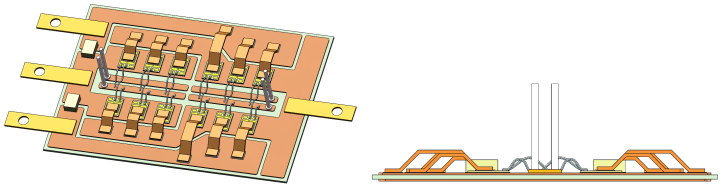
DBC Layout Optimization of Cu Clip-Bonded SiC Power Module and Simulation Verification

TABLE I
Value of equivalent power source parasitic inductances

	Initial	Optimized
L_{e4}/nH	22.55	22.82
L_{e5}/nH	24.64	23.42
L_{e6}/nH	25.22	23.86



(a) Overall view. (b) Side view.

Fig. 3. The DBC layout of the optimized Cu clip-bonded SiC power module.

TABLE II
The main structural parameters of cu clips

Die	Span	Height	Thickness	Corner angle
M_4	16mm	2.5mm	0.5mm	135°
M_5	13mm	2mm	0.5mm	135°
M_6	12.5mm	2mm	0.5mm	135°

DBC Layout Optimization

- Before optimizing the Cu clip-bonded SiC Power Module, the self- and mutual inductance of the initial baseline power module are firstly extracted by ANSYS Q3D;
- The spans, heights, thicknesses and corner angles of the Cu clips of dies M_4-M_6 are rationally adjusted to increase L_{e4} and decrease L_{e5} and L_{e6};
- **The equivalent power source parasitic inductance imbalance degree before and after optimization is 11.06% and 4.45%**, respectively, and the maximum equivalent power source parasitic inductance is reduced by 1.36 nH.

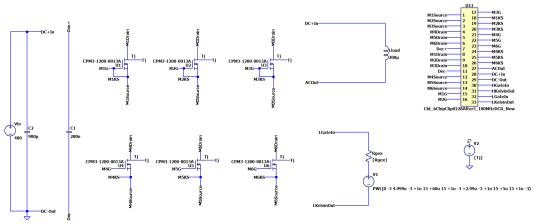
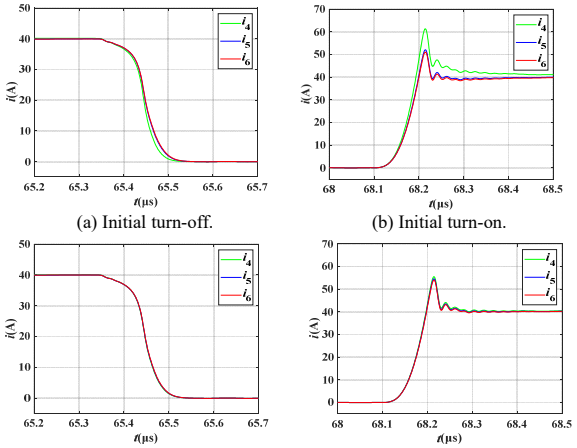


Fig. 4. The double pulse test circuit built in LTspice.



(a) Initial turn-off. (b) Initial turn-on.
(c) Optimized turn-off. (d) Optimized turn-on.

Fig. 5. Simulation waveforms of M_4-M_6 drain current at switching transients.

Simulation Verification

- **The double pulse test circuit** built in LTspice includes the DC voltage source (400V), bus capacitance (900μF), decoupling capacitance (200nF), load inductor (200μH), gate resistance (10Ω), gate drive voltage source (+15V/ -3V);
- The maximum **initial turn-on peak current** difference is 10.30A with an imbalance degree of **18.77%**;
- **After optimization**, **the maximum turn-on peak current** difference is 1.54A and the imbalance degree is as low as **2.81%**.

Conclusion

This article presents an optimization method for dynamic current balancing of paralleled dies in Cu clip-bonded SiC power module. Particularly, based on the self- and mutual inductance of several main current path segments dominated by layout, a parasitic inductance equivalent circuit model at switching transients is established, and a dynamic current balancing guideline is determined. The equivalent power source parasitic inductances are optimized by adjusting the bonding positions and shape parameters of Cu clips. The simulation results demonstrate that the optimized power module has a balanced switching current with an imbalance degree of 2.81% at turn-on (18.77% before optimization), which verifies the effectiveness of the proposed model and optimization method. Future work will mainly focus on improving the reliability of Cu clip-bonding in SiC power module.